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(54) **DISPLAY PANEL AND METHOD FOR DRIVING THE DISPLAY PANEL**

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H01L 27/15 (2006.01)
G09G 3/32 (2016.01)

(52) **U.S. Cl.**

CPC ***G09G 3/2011*** (2013.01); ***G09G 3/2003*** (2013.01); ***G09G 3/2014*** (2013.01);

(Continued)

(58) **Field of Classification Search**

CPC .. G09G 3/2011; G09G 3/2003; G09G 3/2014; G09G 3/32; G09G 2300/0426;

(Continued)

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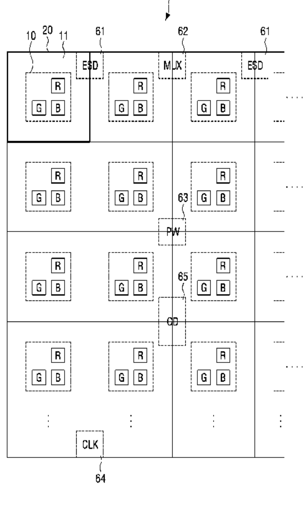
(57) **ABSTRACT**

A display panel is provided. In the display panel, a plurality of pixels respectively including a plurality of sub pixels are arranged in a matrix form on a glass. Each of the plurality of sub pixels includes a driving circuit disposed on the glass and configured to receive a PAM data voltage and a PWM data voltage, and an inorganic light emitting device configured to emit a light based on a driving current provided from the driving circuit. The PAM data voltage is applied at once to the plurality of pixels included in the display panel. The driving circuit compensates a deviation between driving circuits included in each of the plurality of sub pixels based on a driving voltage of the driving circuit, and controls a

(Continued)



pulse width of a driving current having an amplitude corresponding to the applied PAM data voltage based on the applied PWM data voltage.

20 Claims, 17 Drawing Sheets

(52) **U.S. Cl.**
CPC ***G09G 3/32*** (2013.01); ***H01L 27/156*** (2013.01); *G09G 2300/043* (2013.01); *G09G 2300/0426* (2013.01); *G09G 2300/0452* (2013.01); *G09G 2300/0819* (2013.01); *G09G 2310/0202* (2013.01); *G09G 2310/08* (2013.01); *G09G 2320/0633* (2013.01)

(58) **Field of Classification Search**
CPC G09G 2310/0202; G09G 2300/043; G09G 2300/0819; G09G 2300/0452; G09G 2320/0633; G09G 2310/08; H01L 27/156
See application file for complete search history.

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Written Opinion (PCT/ISA/237) dated Jul. 3, 2019 issued by the International Searching Authority in International Application No. PCT/KR2019/001343.
International Search Report (PCT/ISA/210) dated Jul. 3, 2019 issued by the International Searching Authority in International Application No. PCT/KR2019/001357.
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FIG. 1

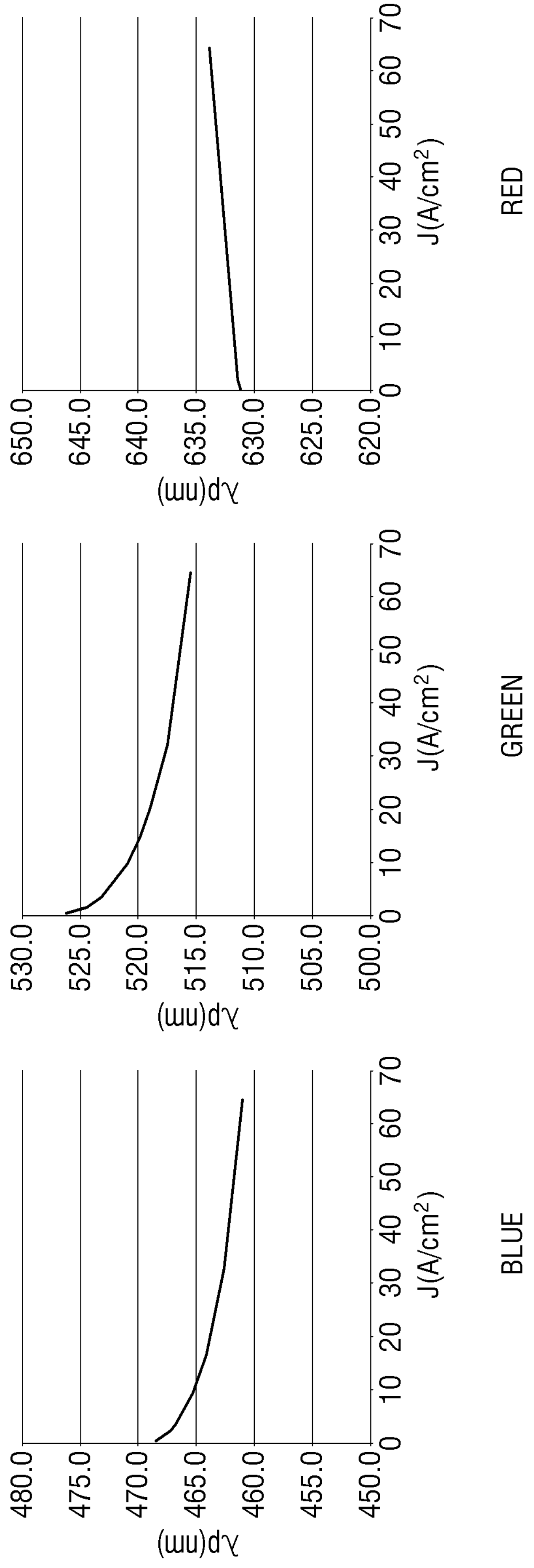

λp(nm)
650.0
645.0
640.0
635.0
630.0
625.0
620.0
0
10
20
30
40
50
60
70
J(A/cm2)
RED
λp(nm)
530.0
525.0
520.0
515.0
510.0
505.0
500.0
0
10
20
30
40
50
60
70
J(A/cm2)
GREEN
λp(nm)
480.0
475.0
470.0
465.0
460.0
455.0
450.0
0
10
20
30
40
50
60
70
J(A/cm2)
BLUE

FIG. 2A

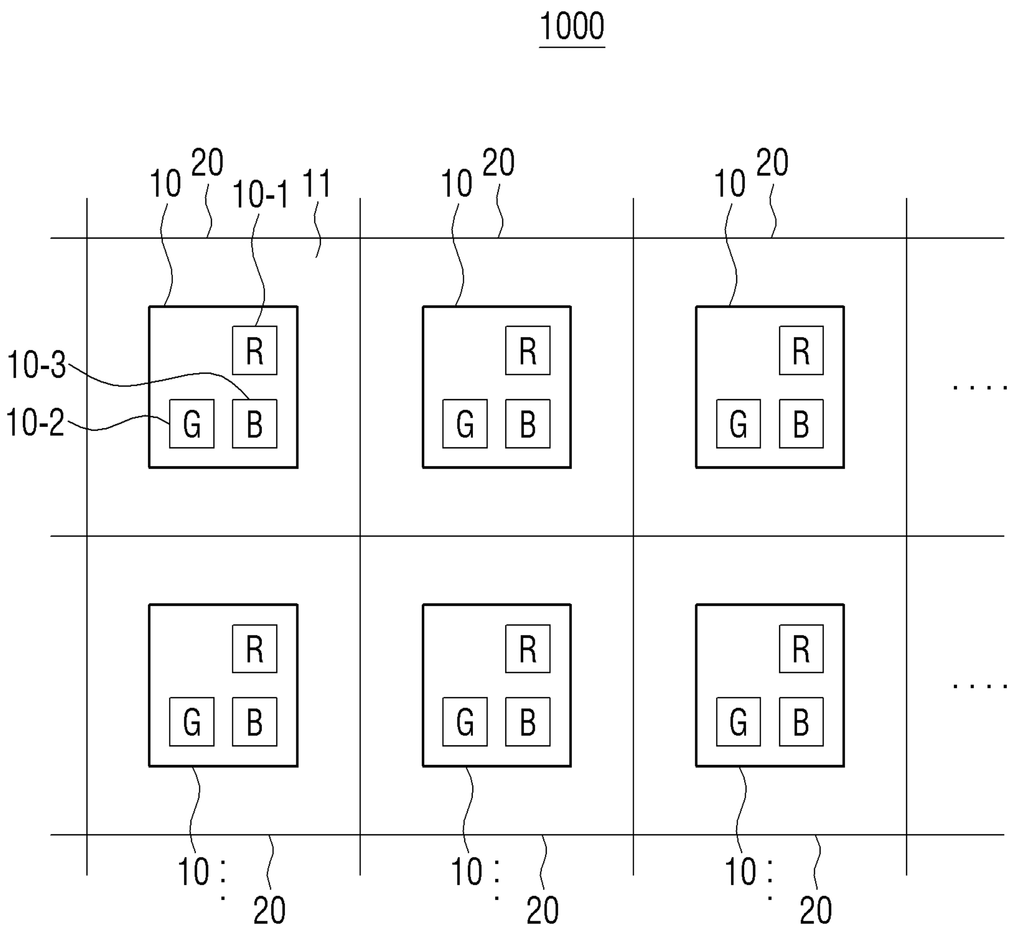

1000
10
20
10-1
11
10
20
10
20
10-3
10-2
R
G
B
R
G
B
R
G
B
....
R
G
B
R
G
B
R
G
B
....
10
20
10
20
10
20

FIG. 2B

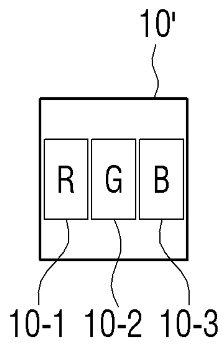


FIG. 3

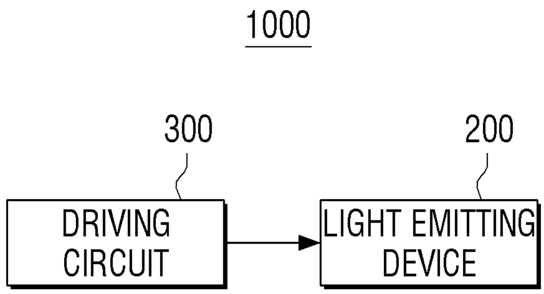


FIG. 4

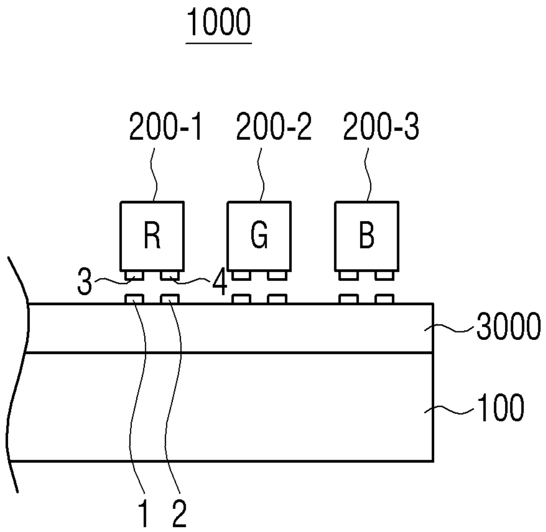


FIG. 5

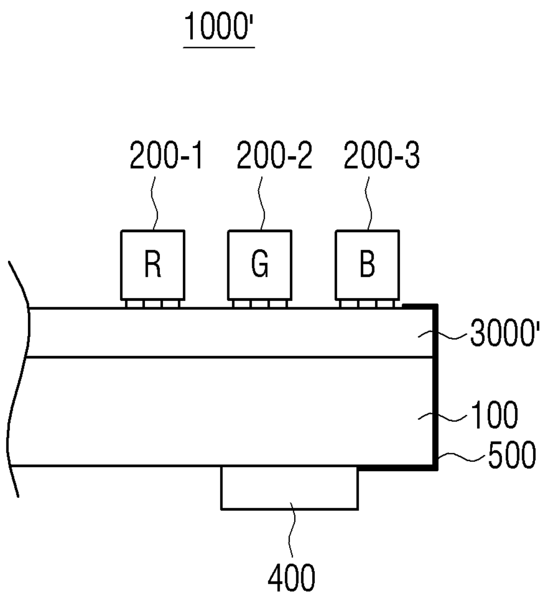


FIG. 6

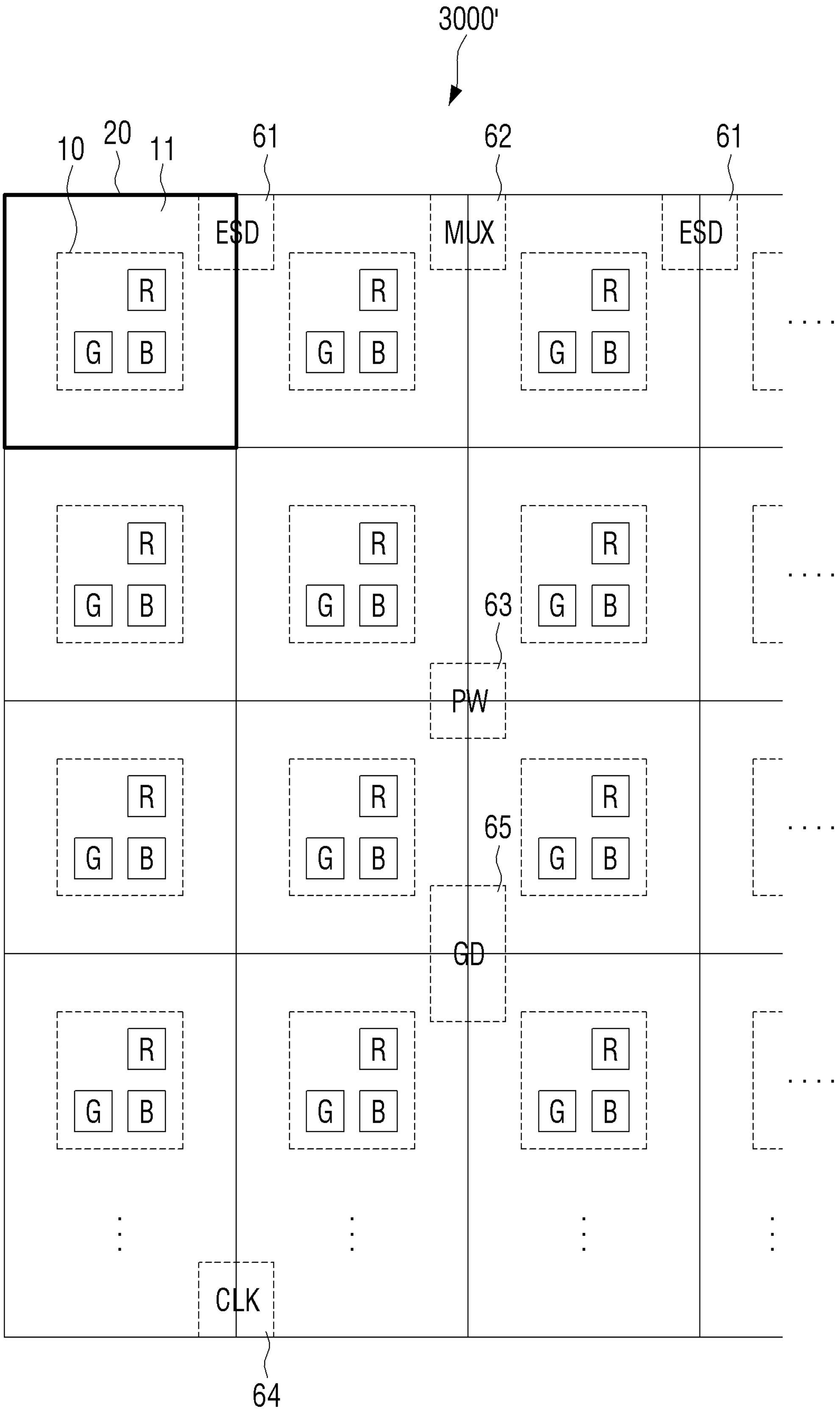


FIG. 7

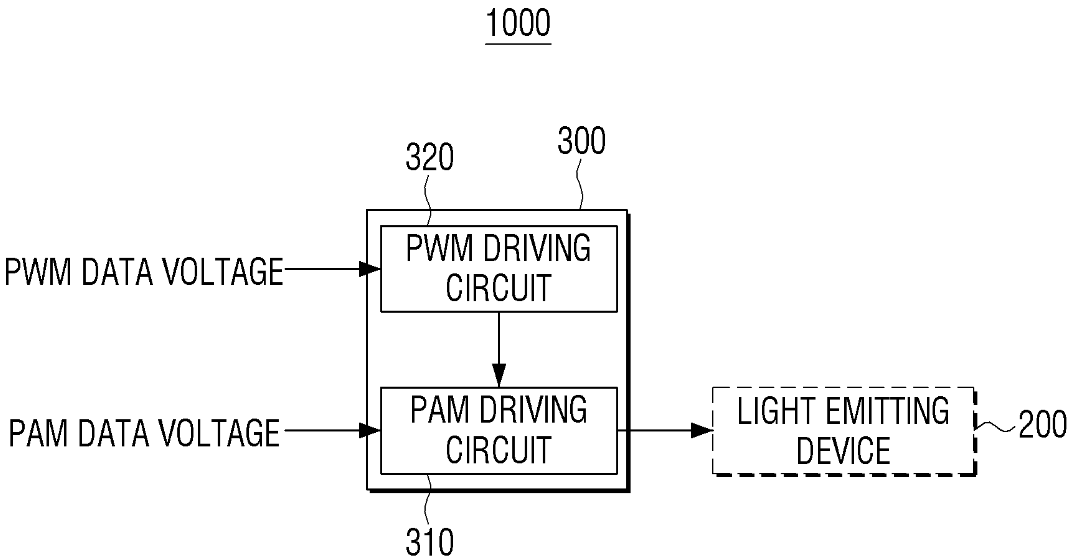

1000
320
300
PWM DATA VOLTAGE
PWM DRIVING CIRCUIT
PAM DATA VOLTAGE
PAM DRIVING CIRCUIT
LIGHT EMITTING DEVICE
200
310

FIG. 8

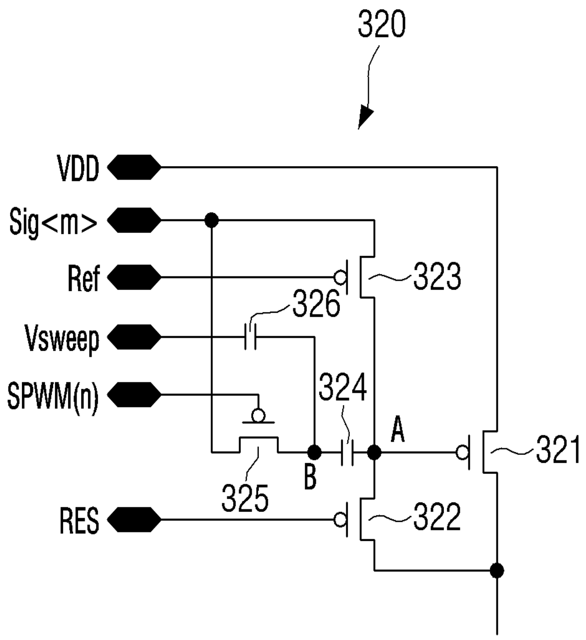
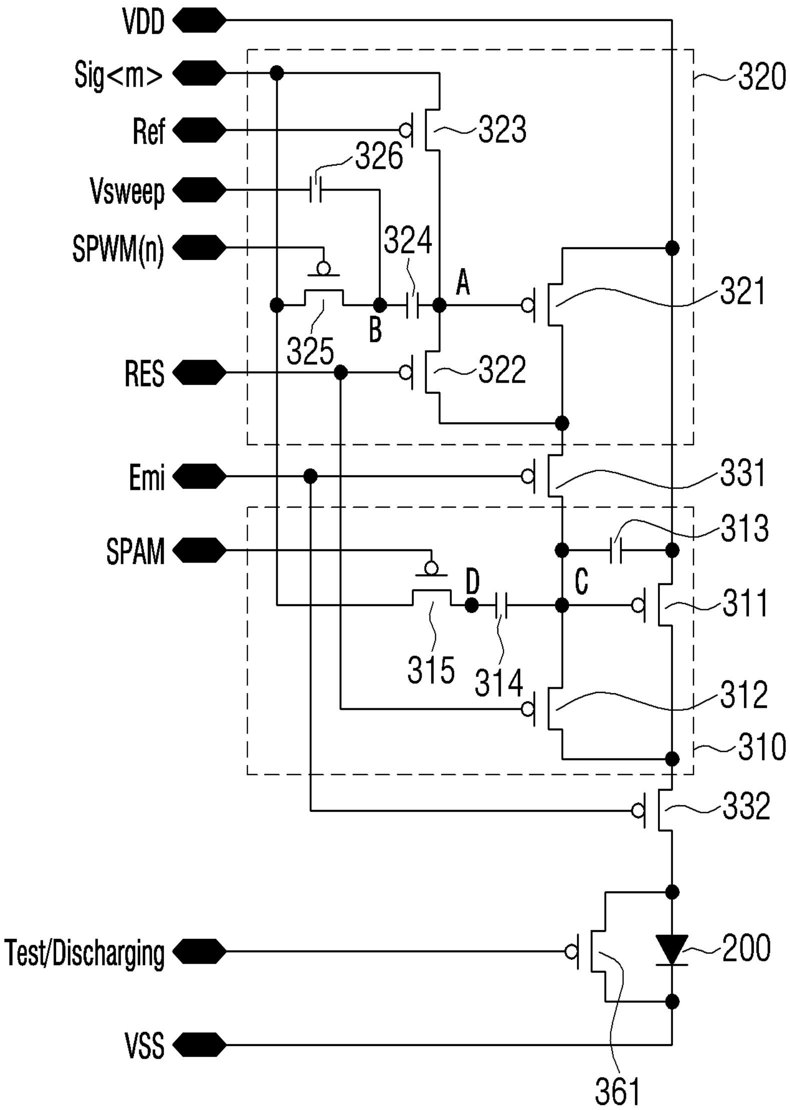


FIG. 9



VDD
Sig<m>
Ref
Vsweep
SPWM(n)
RES
Emi
SPAM
Test/Discharging
VSS
320
323
326
324
A
321
325
B
322
331
313
D
C
311
315
314
312
310
332
200
361

FIG. 10

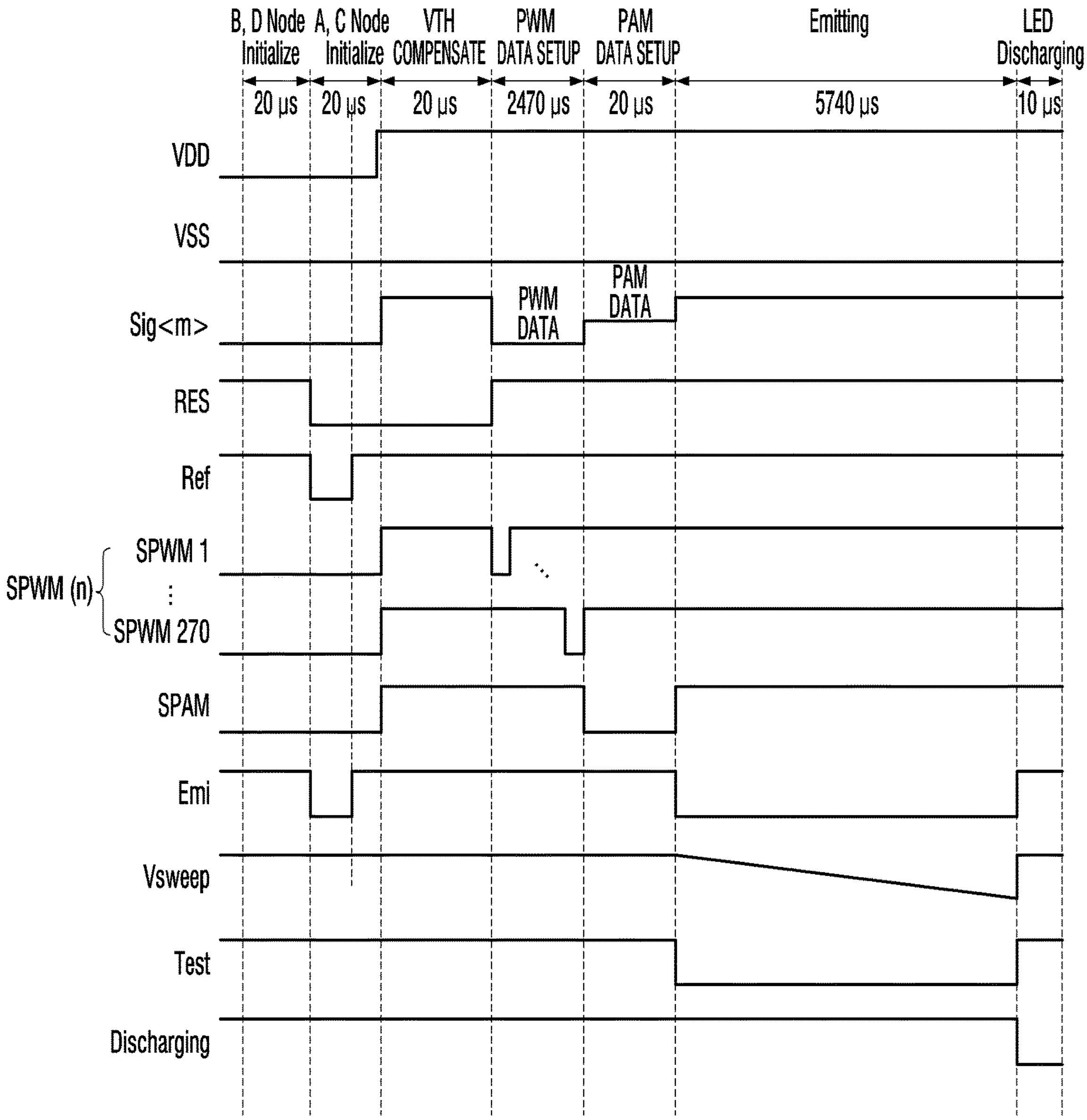
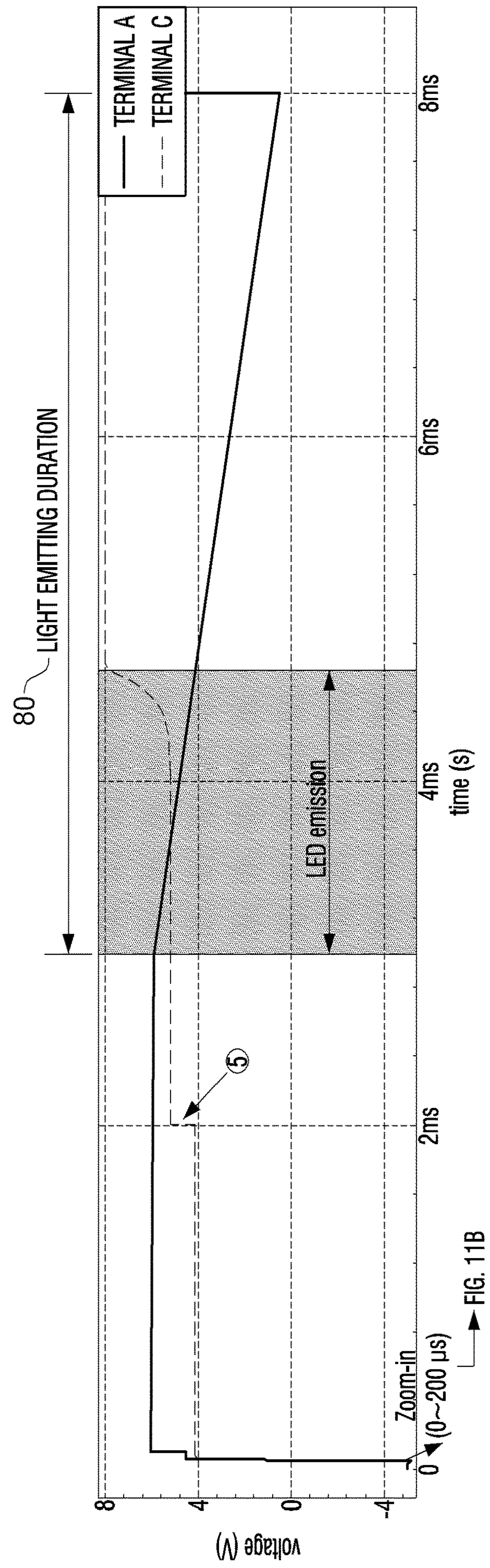

B, D Node Initialize
A, C Node Initialize
VTH COMPENSATE
PWM DATA SETUP
PAM DATA SETUP
Emitting
LED Discharging
20 μs
20 μs
20 μs
2470 μs
20 μs
5740 μs
10 μs
VDD
VSS
Sig<m>
PWM DATA
PAM DATA
RES
Ref
SPWM (n)
SPWM 1
SPWM 270
SPAM
Emi
Vsweep
Test
Discharging

FIG. 11A



TERMINAL A
TERMINAL C
80
LIGHT EMITTING DURATION
LED emission
5
voltage (V)
8
4
0
-4
0
2ms
4ms
6ms
8ms
time (s)
Zoom-in
(0~200 μs)
FIG. 11B

FIG. 11B

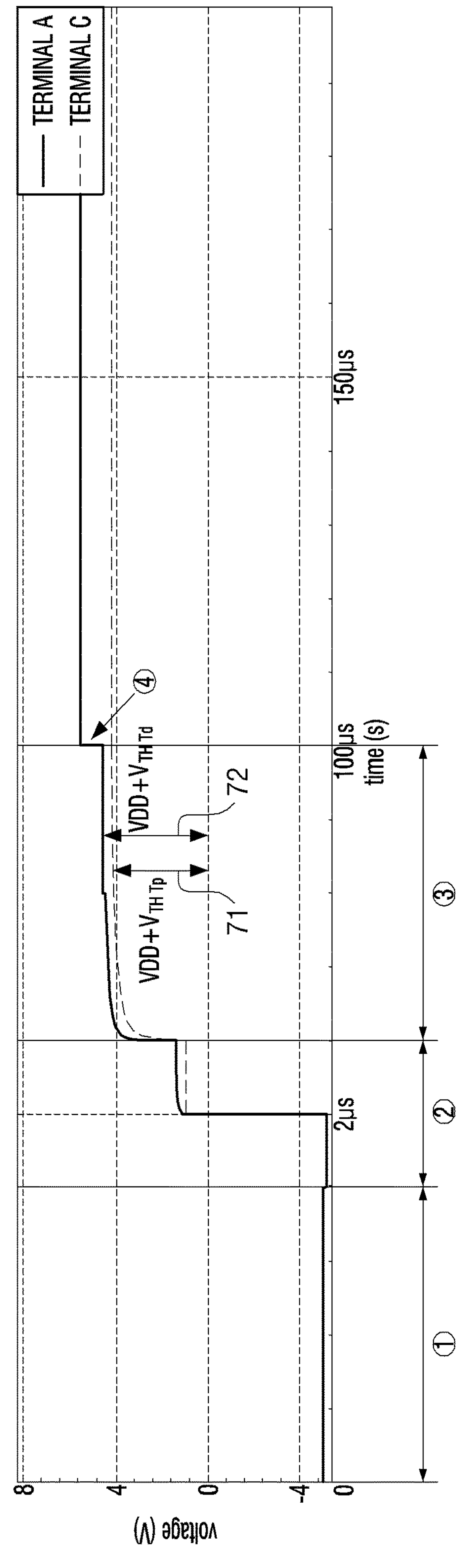

TERMINAL A
TERMINAL C
voltage (V)
8
4
0
-4
0
2μs
100μs
150μs
time (s)
VDD+V_TH Tp
VDD+V_TH Td
71
72
①
②
③
④

FIG. 12A

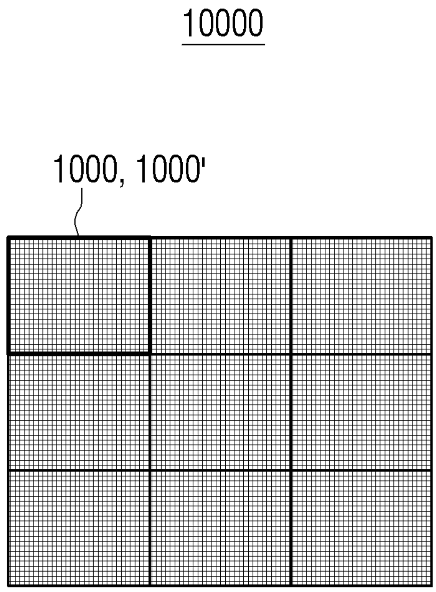
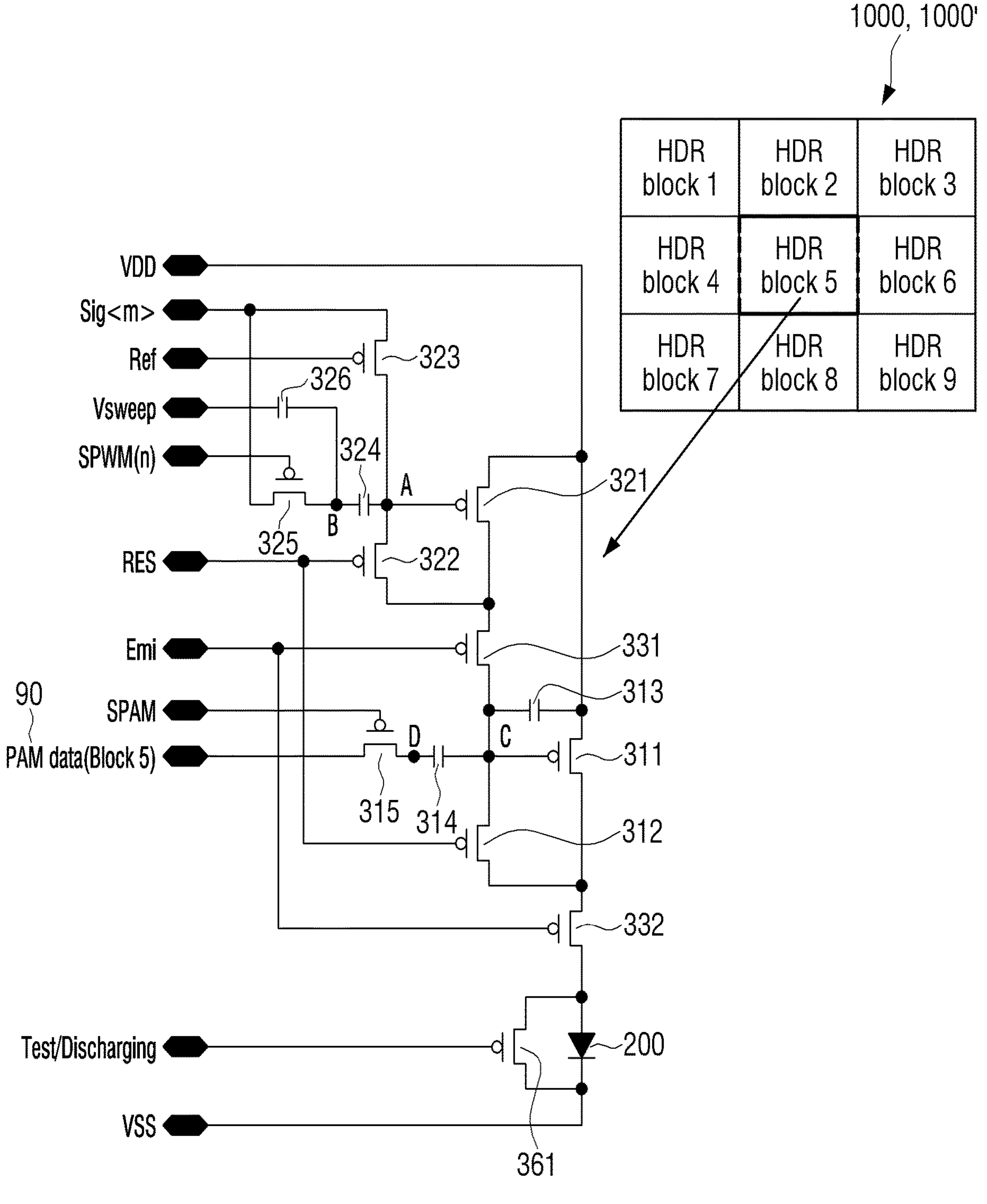


FIG. 12B



1000, 1000'
HDR block 1
HDR block 2
HDR block 3
HDR block 4
HDR block 5
HDR block 6
HDR block 7
HDR block 8
HDR block 9
VDD
Sig<m>
Ref
Vsweep
SPWM(n)
RES
Emi
90
SPAM
PAM data(Block 5)
Test/Discharging
VSS
323
326
324
A
B
325
321
322
331
313
C
D
311
315
314
312
332
200
361

FIG. 13

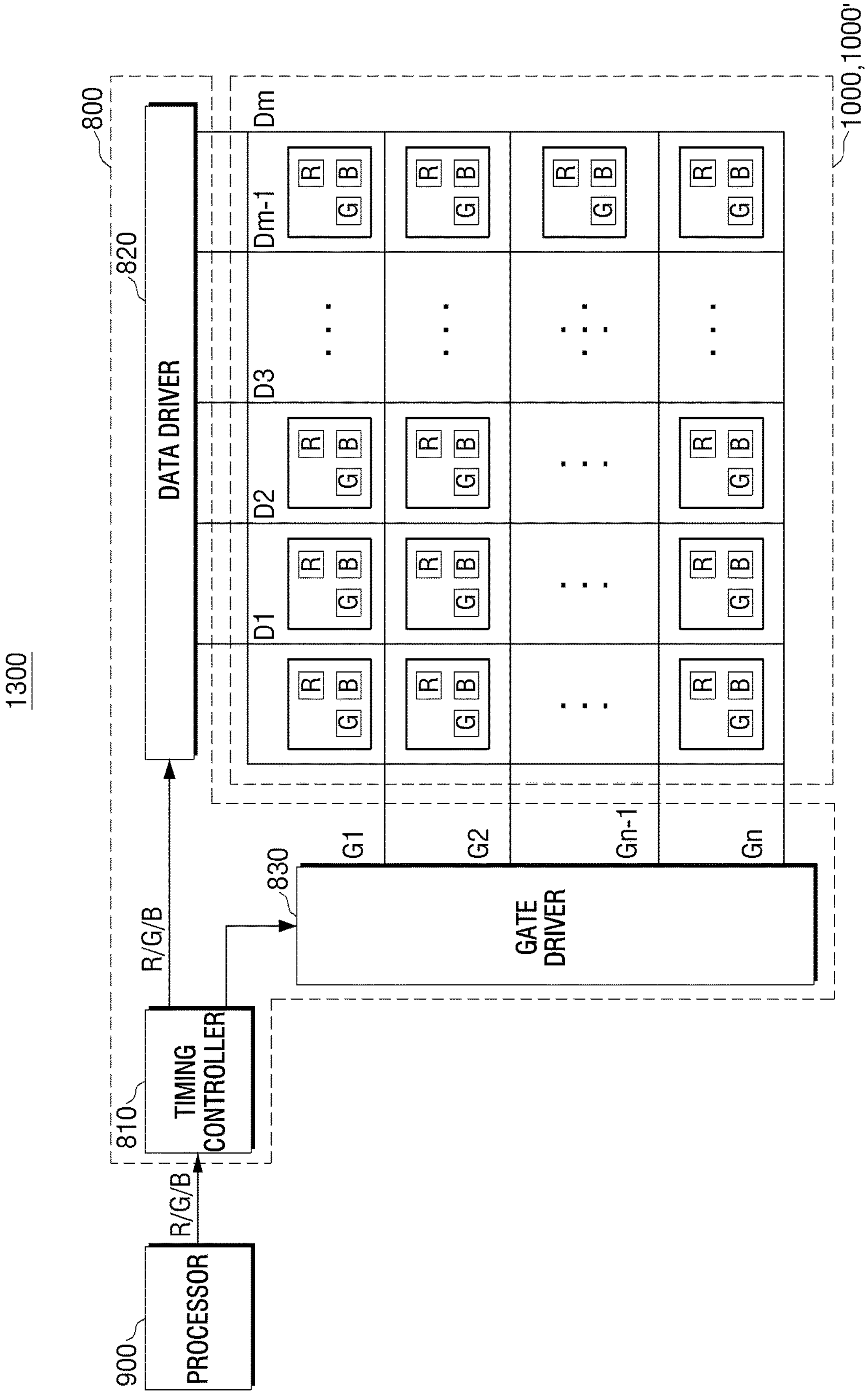
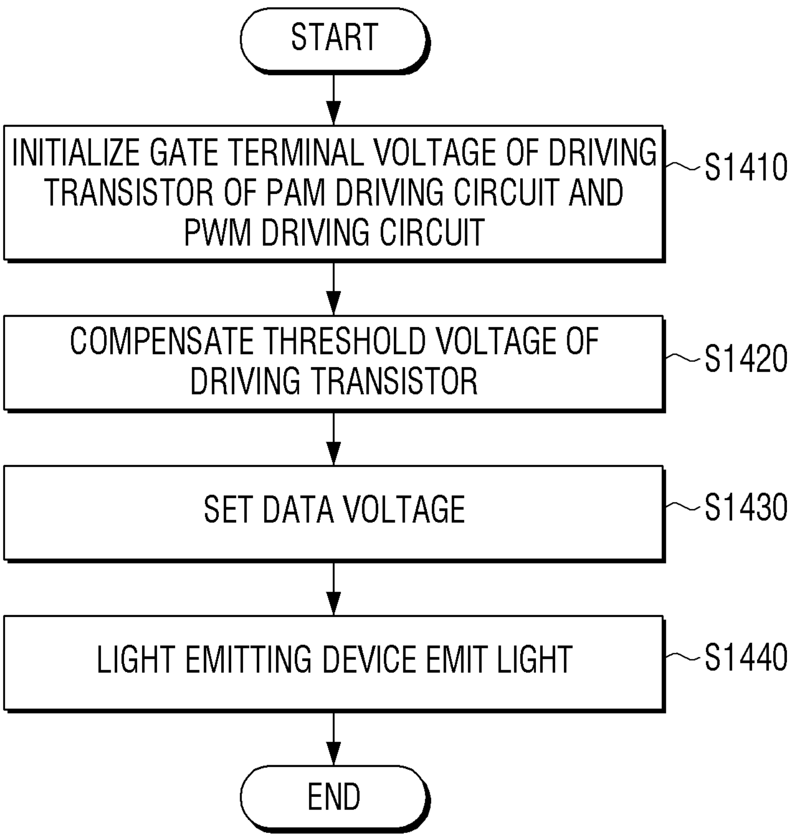

1300
800
820
DATA DRIVER
810
TIMING CONTROLLER
900
PROCESSOR
R/G/B
R/G/B
830
GATE DRIVER
D1
D2
D3
Dm-1
Dm
G1
G2
Gn-1
Gn
R
G
B
1000,1000'

FIG. 14


START
INITIALIZE GATE TERMINAL VOLTAGE OF DRIVING TRANSISTOR OF PAM DRIVING CIRCUIT AND PWM DRIVING CIRCUIT
S1410
COMPENSATE THRESHOLD VOLTAGE OF DRIVING TRANSISTOR
S1420
SET DATA VOLTAGE
S1430
LIGHT EMITTING DEVICE EMIT LIGHT
S1440
END

DISPLAY PANEL AND METHOD FOR DRIVING THE DISPLAY PANEL

CROSS-REFERENCE TO RELATED APPLICATION

This application is based on and claims priority under 35 U.S.C. § 119(a) of a Korean Patent Application number 10-2018-0118317, filed on Oct. 4, 2018, in the Korean Intellectual Property Office, and the disclosure of which is incorporated by reference herein in its entirety.

BACKGROUND

1. Field

The disclosure relates to a display panel and a method for driving the display panel. More particularly, the disclosure relates to a display panel in which light emitting devices are included in a pixel, and a method for driving the display panel.

2. Description of Related Art

In related art, a display panel driving an inorganic light emitting device (hereinafter referred to as "LED") such as a red LED, a green LED, and a blue LED, as a sub pixel expresses a grayscale or gradation of a sub pixel through a pulse amplitude modulation (PAM) drive method.

In this case, a wavelength as well as a grayscale or gradation of a light emitted is shifted together according to an amplitude of the driving current, and thereby a color reproducibility of an image is reduced. FIG. **1** illustrates wavelength shifts according to a magnitude or an amplitude of a driving current flowing through a blue LED, a green LED, and a red LED.

The above information is presented as background information only to assist with an understanding of the disclosure. No determination has been made, and no assertion is made as to whether any of the above description may be applicable as prior art with regard to the disclosure.

SUMMARY

Aspects of the disclosure are to address at least the above-mentioned problems and/or disadvantages and to provide at least the advantages described below. Accordingly, an aspect of the disclosure is to provide a display panel providing improved color reproducibility to an input image signal through an LED which is an inorganic light emitting device mounted on a glass substrate, and a method for driving the display panel.

Another aspect of the disclosure is to provide a display panel including a driving circuit capable of more efficiently driving an LED which is an inorganic light emitting device mounted on a glass substrate, and a method for driving the display panel.

Another aspect of the disclosure is to provide a display panel including a driving circuit appropriate for a high-density integrated circuit by optimizing a design of a driving circuit driving an LED which is an inorganic light emitting device mounted on a glass substrate, and a method for driving the display panel.

Another aspect of the disclosure is to provide a display panel including a driving circuit capable of stably operating an LED which is an inorganic light emitting device mounted on a glass substrate, and a method for driving the display panel.

In accordance with an aspect of the disclosure, a display panel is provided. In the display panel, a plurality of pixels respectively including a plurality of sub pixels are arranged in a matrix form on a glass. Each of the plurality of sub pixels includes a driving circuit disposed on the glass and configured to receive a pulse amplitude modulation (PAM) data voltage and a pulse width modulation (PWM) data voltage, and an inorganic light emitting device mounted on the driving circuit and configured to be electrically connected to the driving circuit, and to emit a light based on a driving current provided from the driving circuit. The PAM data voltage is applied at once to the plurality of pixels included in the display panel. The driving circuit is configured to control a grayscale of a light emitted by the inorganic light emitting device by compensating a deviation between driving circuits included in each of the plurality of sub pixels based on a driving voltage of the driving circuit and controlling a pulse width of a driving current having an amplitude corresponding to the applied PAM data voltage based on the applied PWM data voltage.

The driving circuit may include a PAM driving circuit including a first driving transistor and configured to control amplitude of the driving current based on the applied PAM data voltage, and a PWM driving circuit including a second driving transistor and configured to control a pulse width of the driving current based on the applied PWM data voltage. The deviation between the driving circuits may be a deviation of threshold voltage between first driving transistors included in each of the plurality of sub pixels, and a deviation of threshold voltage between second driving transistors included in each of the plurality of sub pixels.

The PAM driving circuit may be configured to, based on the driving voltage being applied, apply a first voltage based on the driving voltage and a threshold voltage of the first driving transistor to a gate terminal of the first driving transistor. The PWM driving circuit may be configured to, based on the driving voltage being applied, apply a second voltage based on the driving voltage and a threshold voltage of the second driving transistor to a gate terminal of the second driving transistor.

The PAM driving circuit may be configured to, after a gate terminal voltage of the first driving transistor being equal to the first voltage, based on the PAM data voltage being applied, apply a third voltage based on the first voltage and the PAM data voltage to the gate terminal of the first driving transistor. The PWM driving circuit may be configured to, after a gate terminal voltage of the second driving transistor being equal to the first voltage, based on the PWM data voltage being applied, apply a fourth voltage based on the second voltage and the PWM data voltage to the gate terminal of the second driving transistor. The driving circuit may be configured to, based on the driving voltage being applied to the inorganic light emitting device through the first driving transistor and a linearly-changing sweep signal being applied to the PWM driving circuit, provide a driving current of an amplitude corresponding to the applied PAM data voltage to the inorganic light emitting device from a time when the driving voltage is applied to the inorganic light emitting device until a time when the fourth voltage applied to the gate terminal of the second driving transistor is linearly shifted according to the sweep signal and becomes the second voltage.

The PWM data voltage may be sequentially applied to the plurality of pixels for each line of the plurality of pixels arranged in the matrix form.

The PAM data voltage applied at once to the plurality of sub pixels may be a voltage of the same magnitude.

The display panel may be divided into a plurality of areas. The PAM driving circuit may receive the PAM data voltage for each of the plurality of areas.

A PAM data voltage applied to at least one area for driving a high dynamic range (HDR) from among the plurality of areas may be different from a PAM data voltage applied to other areas of the plurality of areas.

The plurality of sub pixels may include an R sub pixel including an inorganic light emitting device emitting a red (R) light, a G sub pixel including an inorganic light emitting device emitting a green (G) light, and a B sub pixel including an inorganic light emitting device emitting a blue (B) light.

The inorganic light emitting device may be a micro-LED (micro Light Emitting Diode) having a magnitude of less than or equal to 100 micrometers.

The PAM driving circuit may include a first transistor which is connected to and disposed between a drain terminal of the first driving transistor and the gate terminal of the first driving transistor, a first capacitor including a first terminal commonly connected to a source terminal of the first driving transistor, a source terminal of the second driving transistor, and a driving voltage terminal of the driving circuit, a second capacitor including a first terminal commonly connected to the gate terminal of the first driving transistor, a second terminal of the first capacitor, and a source terminal of the first transistor, and a second transistor including a source terminal via which the PAM data voltage is applied, and a drain terminal connected to a second terminal of the second capacitor.

The PAM driving circuit may be configured to, while the first transistor is turned on, based on the driving voltage being applied via the driving voltage terminal, apply the first voltage corresponding to a sum of the driving voltage and the threshold voltage of the first driving transistor to the gate terminal of the first driving transistor via the turned-on first driving transistor, and based on the PAM data voltage being applied via the source terminal of the second transistor, to apply the third voltage corresponding to a sum of the first voltage and the applied PAM data voltage to a gate terminal of the first transistor.

The PWM driving circuit may include a third transistor which is connected to in between a drain terminal of the second driving transistor and the gate terminal of the second driving transistor, a fourth transistor including a drain terminal connected to the gate terminal of the second driving transistor and a source terminal of the third transistor, a third capacitor including a first terminal commonly connected to the gate terminal of the second driving transistor, the source terminal of the third transistor, and the drain terminal of the fourth transistor, a fifth transistor including a source terminal via which the PWM data voltage is applied, and a drain terminal connected to a second terminal of the third capacitor, and a fourth capacitor including a first terminal commonly connected to the second terminal of the third capacitor and the drain terminal of the fifth transistor, and a second terminal receiving a linearly-shifting sweep signal.

The PWM driving circuit may be configured to, while the third transistor is turned on, based on the driving voltage being applied via a the driving voltage terminal, apply the second voltage corresponding to a sum of the driving voltage and the threshold voltage of the second driving transistor to the gate terminal of the second driving transistor via the turned-on second driving transistor, and based on the PWM data voltage being applied via the source terminal of the fifth transistor, to apply the fourth voltage corresponding to the second voltage and the applied PWM data voltage to the gate terminal of the second transistor.

The driving circuit may further include a sixth transistor including a source terminal commonly connected to the drain terminal of the second driving transistor and a drain terminal of the third transistor, and a drain terminal commonly connected to the gate terminal of the first driving transistor, the second terminal of the first capacitor, the first terminal of the second capacitor, and the source terminal of the first transistor, and a seventh transistor including a source terminal commonly connected to the drain terminal of the first driving transistor and a drain terminal of the first transistor, and a drain terminal connected to an anode terminal of the light emitting device. A cathode terminal of the inorganic light emitting device may be connected to a ground voltage terminal of the driving circuit.

The driving circuit may be configured to drive the PAM driving circuit and the PWM driving circuit independently of each other while the sixth and seventh transistors are turned off, and apply the first voltage and the second voltage to the gate terminal of the first driving transistor and the gate terminal of the second driving transistor, respectively, and while the sixth and seventh transistors are turned on, based on the sweep signal being applied via the fourth capacitor, to drive the PAM driving circuit and the PWM driving circuit together, and until the fourth voltage applied to the gate terminal of the second driving transistor is shifted according to the sweep voltage and becomes the second voltage, provide a driving current of an amplitude corresponding to the applied PAM data voltage to the inorganic light emitting device.

Gate terminal voltages of the first and second driving transistors may be, before the first and second voltages are respectively applied, initialized based on an initial voltage applied via the fourth transistor turned on while the sixth and seventh transistors are turned on.

The driving circuit may further include an eighth transistor which is connected to and disposed between an anode terminal of the inorganic light emitting device and a cathode terminal of the inorganic light emitting device.

The eighth transistor may be configured to, before the inorganic light emitting device is mounted on the driving circuit, be turned on to check whether the driving circuit is abnormal, and after the inorganic light emitting device is mounted on the driving circuit, to be turned on to discharge an electric charge remaining in the inorganic light emitting device.

In accordance with another aspect of the disclosure, a method for driving a display panel is provided. In the display panel, a plurality of pixels respectively including a plurality of sub pixels are arranged in a matrix form on a glass. Each of the plurality of sub pixels includes a driving circuit formed on the glass and configured to receive a pulse amplitude modulation (PAM) data voltage and a pulse width modulation (PWM) data voltage, and an inorganic light emitting device mounted on the driving circuit to be electrically connected to the driving circuit, and configured to emit a light based on a driving current provided from the driving circuit. The method includes compensating a threshold voltage of a driving transistor included in the driving circuit based on a driving voltage of the driving circuit, setting the applied PAM data voltage and the applied PWM data voltage, and providing, to the inorganic light emitting device, a driving current having an amplitude corresponding to the applied PAM data voltage and a pulse width corresponding to the applied PWM data voltage. The PAM data voltage is applied at once to the plurality of pixels included in the display panel.

According to the various example embodiments, a wavelength shift of a light emitted from an inorganic light emitting device included in a display panel according to a grayscale or gradation can be prevented.

In addition, it is possible to correct a stain or color of the light emitting device included in the display panel, and even in a case that a large-area tiled display panel is configured by combining a display panel in the form of a plurality of modules, a difference of brightness or color among the respective modular display panels can be corrected.

Further, a more optimized driving circuit design is enabled so that the inorganic light emitting device can be driven more stably and efficiently, thereby contributing to a miniaturization and lightening of a display panel.

Other aspects, advantages, and salient features of the disclosure will become apparent to those skilled in the art from the following detailed description, which, taken in conjunction with the annexed drawings, discloses various embodiments of the disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other aspects, and advantages of certain embodiments of the disclosure will be more apparent from the following description taken in conjunction with the accompanying drawings, in which:

FIG. **1** is a diagram illustrating a wavelength shift according to a magnitude of a driving current flowing through a blue LED, a green LED, and a red LED;

FIG. **2**A is a diagram illustrating a pixel structure of a display panel, according to an example embodiment;

FIG. **2**B is a diagram illustrating a sub-pixel structure, according to another example embodiment;

FIG. **3** is a block diagram illustrating a configuration of a display panel, according to an example embodiment;

FIG. **4** is a cross-sectional view of a display panel, according to an example embodiment;

FIG. **5** is a cross-sectional view of a display panel, according to another example embodiment;

FIG. **6** is a plane view illustrating a thin film transistor (TFT) layer, according to an example embodiment;

FIG. **7** is a block diagram and circuit diagram related to one sub pixel, according to an example embodiment;

FIG. **8** is a circuit diagram of a pulse width modulation (PWM) driving circuit, according to an example embodiment;

FIG. **9** is a detailed circuit diagram of a driving circuit, according to an example embodiment;

FIG. **10** is a timing diagram of various signals for driving a driving circuit of FIG. **9**, according to an example embodiment;

FIGS. **11**A and **11**B are experiment waveforms for nodes A and C of a driving circuit, according to an example embodiment;

FIGS. **12**A and **12**B are diagrams illustrating a high dynamic range (HDR) realized through a display panel, according to an example embodiment;

FIG. **13** is a diagram illustrating a configuration of a display apparatus, according to an example embodiment; and

FIG. **14** is a flowchart illustrating a method for driving a display apparatus, according to an example embodiment.

The same reference numerals are used to represent the same elements throughout the drawings.

DETAILED DESCRIPTION

In the following description, well-known functions or constructions are not described in detail since they would obscure the application with unnecessary detail. In addition, the overlapped description of the same element is omitted as much as possible.

The term "unit" is provided or mixed up in use for the ease of preparing the present specification, which does not itself have a distinct meaning or serve a purpose.

The terms used in the following description are provided to explain example embodiments and are not intended to limit the scope. It is to be understood that the singular forms "a," "an," and "the" include plural referents unless the context clearly dictates otherwise.

Throughout this specification, it will be understood that the term "comprise" and variations thereof, such as "comprising" and "comprises", specify the presence of features, numbers, steps, operations, components, parts, or combinations thereof, described in the specification, but do not preclude the presence or addition of one or more other features, numbers, steps, operations, components, parts, or combinations thereof.

In the description, the terms "first, second, and so forth" are used to describe diverse elements regardless of their order and/or importance and to discriminate one element from other elements, but are not limited to the corresponding elements.

If it is described that a certain element (e.g., first element) is "operatively or communicatively coupled with/to" or is "connected to" another element (e.g., second element), it should be understood that the certain element may be connected to the other element directly or through still another element (e.g., third element). Meanwhile, when it is mentioned that one element (e.g., first element) is "directly coupled" with or "directly connected to" another element (e.g., second element), it may be understood that there is no element (e.g., third element) present between the element and the other element.

Unless indicated otherwise, it is to be understood that all the terms used in the disclosure including technical and scientific terms has the same meaning as those that are understood by those who skilled in the art.

Hereinafter, the disclosure will be described in detail with reference to the accompanying drawings.

FIG. **2**A is a diagram illustrating a pixel structure of a display panel **1000**, according to an example embodiment. As illustrated in FIG. **2**A, the display panel **1000** may include a plurality of pixels **10** which are arranged in a matrix form.

The respective pixels **10** may include a plurality of sub-pixels **10-1**, **10-2** and **10-3**. For example, one pixel **10** included in the display panel **1000** may include three types of sub-pixels: a red (R) sub-pixel **10-1**, a green (G) sub-pixel **10-2**, and a blue (B) sub-pixel **10-3**. That is, one set of R, G and B sub-pixels may constitute a unit pixel of the display panel **1000**.

Referring to FIG. **2**A, it may be understood that one pixel area **20** of the display panel **1000** may include an area **10** occupied with pixels, and a remaining peripheral area **11**.

The area **10** occupied with pixels **10** may include the R, G and B sub-pixels **10-1** to **10-3**. The R sub-pixel **10-1** may include an R light emitting device and a driving circuit for driving the R light emitting device. The G sub-pixel **10-2** may include a G light emitting device and a driving circuit for driving the G light emitting device. The B sub-pixel **10-3** may include a B light emitting device and a driving circuit for driving the B light emitting device.

The remaining area **11** peripheral to the pixel **10** may, as will be described with reference to FIGS. **5** and **6**, include various circuits for driving the driving circuit according to an example embodiment.

FIG. **2**B is a diagram illustrating a sub-pixel structure, according to another example embodiment. Referring to FIG. **2**A, it may be understood that the sub-pixels **10-1** to **10-3** in the one pixel **10** are arranged in an L shape of which the left and right side are switched. However, the example is not limited thereto, and as illustrated in FIG. **2**B, the R, G and B sub-pixels **10-1** to **10-3** may be arranged in a row inside a pixel **10'**. However, the disposition form of the sub-pixels is only an example, and a plurality of sub-pixels are disposed in various forms inside the respective pixels according to example embodiments.

In the example described above, a pixel includes three types of sub-pixels, but is not limited thereto. For example, a pixel may be implemented of four types such as R, G, B and white (W), and according to an example embodiment, a different number of pixels may be included in one pixel. Hereinafter, an example in which the pixel **10** includes three types of sub-pixels such as R, G and B will be described for convenience of explanation.

FIG. **3** is a block diagram illustrating a configuration of a display panel, according to an example embodiment. Referring to FIG. **3**, the display panel **1000** may include a driving circuit **300** and a light emitting device **200** (or light emitting diode). The display panel **1000** may include a driving circuit **300** disposed on a glass, and a light emitting device **200** disposed on the driving circuit **300** as will be described later.

For example, the light emitting device **200** may be mounted on the driving circuit **300** so that the light emitting device **200** is electrically connected to the driving circuit **300**, and may emit light on the basis of a driving current provided from the driving circuit **300**.

The light emission device **200** may be included in the sub-pixels **10-1** to **10-3** of the display panel **1000**, and may be of a plurality of types according to a color of light. For example, the light emitting device **200** may include a red (R) light emitting device emitting light in red color, a green (G) light emitting device emitting light in green light, and a blue (B) light emitting device emitting light in blue color.

Accordingly, a type of sub-pixel may be determined according to a type of the light emitting device **200** included in the sub-pixel. That is, the R light emitting device may be included in the R sub-pixel **10-1**. The G light emitting device may be included in the G sub-pixel **10-2**. The B light emitting device may be included in the B sub-pixel **10-3**.

The light emitting device **200** may be an inorganic light emitting device (or inorganic light emitting diode) by means of an inorganic material which is different from an organic light emitting device (OLED)(or organic light emitting diode) fabricated using an organic material. Hereinafter, the LED refers to an inorganic light emitting device which is distinguished from the OLED.

According to an example embodiment, the light emitting device **200** may be a micro light emitting diode (micro-LED). The micro LED refers to a subminiature inorganic light emitting device having a size of less than or equal to 100 micrometers (μm) self-illuminating without a backlight or a color filter.

In addition, the light emitting device **200** may emit light according to a driving current provided by the driving circuit **300**. For example, the light emitting device **200** may emit light with different brightnesses according to an amplitude or a pulse width of a driving current provided from the driving circuit **300**. Here, the pulse width of the driving current may be expressed as a duty ratio of the driving current or a driving time of the driving current.

For example, the light emitting device **200** may emit light of a higher brightness with the increase in the amplitude of the driving current and with the increase in the pulse width (that is, with the increase in the duty ratio or with the increase in the driving time). However, the example is not limited thereto.

The driving circuit **300** may drive the light emitting device **200**. For example, the driving circuit **300** may pulse amplitude modulation (PAM) drive or pulse width modulation (PWM) drive the light emitting device **200** to control a grayscale or gradation of a light emitted by the light emitting device **200**.

That is, the driving circuit **300** may, for example, receive application of a PAM data voltage and a PWM data voltage from a data driver (not illustrated) and control an amplitude and pulse width of a driving current driving the light emitting device **200** together, and provide the driving current of which amplitude and pulse width are controlled together to the light emitting device **200**, and drive the light emitting device **200**.

Here, the amplitude and the pulse width of the driving current being controlled "together" does not mean that the driving circuit **300** controls the amplitude and the pulse width of the driving current simultaneously in time, but means that the PAM drive method and the PWM drive method are employed together to express a grayscale or gradation.

The driving circuit **300** may control a pulse width of a driving current having an amplitude corresponding to the applied PAM data voltage on the basis of the applied PWM data voltage.

According to an example embodiment, the driving circuit **300** may compensate a deviation between driving circuits included in each of a plurality of sub pixels based on a driving voltage (VDD) driving the driving circuit **300**.

In addition, the PAM data voltage may be applied at once to all pixels (or all sub pixels) included in the display panel **1000**. A specific description regarding this operation will be explained below.

According to an example embodiment, the driving circuit **300** may drive the light emitting device **200** and express a grayscale or gradation by the sub pixel. As described above, the display panel **1000** may include sub-pixels by the light emitting device **200**, and thus, unlike a liquid crystal display (LCD) panel using a plurality of LEDs emitting light in a single color as a backlight, the driving circuit **300** may drive the light emitting device **200** and differently expresses a grayscale or gradation by the sub-pixel.

To this end, the respective sub-pixels included in the display panel **1000** may include the light emitting device **200** and a driving circuit **300** for driving the corresponding light emitting device **200**. That is, the driving circuit **300** for driving the respective device **200** may be present for each sub-pixel.

The PWM drive method is a method of expressing a grayscale or gradation according to a duration of light emission of the light emitting device **200**. Accordingly, in a case that the light emitting device **200** is driven using the PWM method, even if the driving current has the same amplitude, it is possible to express various grayscales or gradations by adjusting the pulse width of the driving current and controlling the duration of light emission of the light emitting device **200**. Accordingly, it is possible to solve the problem of a wavelength shift of light emitted by an LED (in particular, micro-LED) by driving the LED solely by the PAM method.

To this end, the driving circuit **300** may include a PAM driving circuit and a PWM driving circuit for each sub pixel, and this will be described in greater detail below.

FIG. **4** is a cross-sectional view of a display panel **1000**, according to an example embodiment. With reference to FIG. **4**, only one pixel included in the display panel **1000** is described for convenience of explanation.

Referring to FIG. **4**, the display panel **1000** may include a glass **100**, a thin film transistor (TFT) layer **3000**, and light emitting devices R, G and B **200-1**, **200-2** and **200-3**. The driving circuit **300** (not illustrated) may be implemented as a thin film transistor (TFT) and included in the TFT layer **3000** disposed on the glass **100**. The respective light emitting devices R, G and B **200-1** to **200-3** may be arranged on the TFT layer **3000** and included in the respective sub pixels **10-1** to **10-3** of the display panel **1000**.

As described above, the display panel **1000** in which the TFT layer **3000** and the light emitting devices **200-1** to **200-3** are disposed on the glass **100** may be referred to as a display panel of a chip on glass (COG) type. The display panel of the COG type is different from a display panel of a chip on board (COB) type in which a TFT layer and a light emitting device layer are disposed on a substrate such as a synthetic resin and the like.

In this case, the TFT layer **3000** may be a low temperature poly silicon (LTPS) TFT, but is not limited thereto. Meanwhile, the TFT layer **3000** disposed on the glass **100** and the glass **100** may be added together and referred to as a TFT panel or a glass substrate. A type or characteristic of the glass **100** included in the glass substrate is not related to the example embodiments so that an explanation thereof is omitted.

Although not expressly illustrated in the drawings, the driving circuit **300** for driving the respective light emitting devices **200-1** to **200-3** may be present on the TFT layer **3000** for each of the light emitting devices **200-1** to **200-3**. The light emitting devices R, G and B **200-1** to **200-3** may be arranged on the TFT layer **3000** so that they are respectively electrically connected to the corresponding driving circuit **300**.

For example, as illustrated in FIG. **4**, the R light emitting device **200-1** may be mounted or arranged so that an anode electrode **3** and a cathode electrode **4** of the R light emitting device **200-1** are respectively connected to an anode electrode **1** and a cathode electrode **2** disposed on the driving circuit **300** (not illustrated) for driving the R light emitting device **200-1**, and the same applies to the G light emitting device **200-2** and the B light emitting device **200-3**. According to an example embodiment, any one of the anode electrode **1** and the cathode electrode **2** may be implemented as a common electrode.

With reference to FIG. **4**, an example in which the light emitting device **200-1** to **200-3** is a micro-LED of a flip chip type is described. However, the example is not limited thereto, and according to an example embodiment, the light emitting device **200-1** to **200-3** may be a micro-LED of a lateral type or a micro-LED of a vertical type.

According to an example embodiment, the display panel **1000** may further include a multiplexer (MUX) circuit for selecting any one of the plurality of sub pixels **10-1** to **10-3** included in the pixel **10**, an electro static discharge (ESD) circuit for preventing a static electricity occurring on the display panel **1000**, a power circuit for supplying power to the driving circuit **300**, a clock provision circuit for providing a clock driving the driving circuit **300**, at least one gate driver for driving pixels of the display panel **1000** arranged in a matrix form by the horizontal line (or by the row), a data driver (or a source driver) for providing a data voltage (for example, a PAM data voltage, a PWM data voltage, or the like) to the respective pixels or to the respective sub-pixels, and the like.

An example display panel further comprising these various circuits will be described in greater detail below with reference to FIGS. **5** and **6**. In FIGS. **5** and **6**, the same elements described above will not be described in detail.

FIG. **5** is a cross-sectional view of a display panel **1000'**, according to an example embodiment. As illustrated in FIG. **5**, the display panel **1000'** may include a TFT layer **3000'** including a driving circuit **300** (not illustrated) disposed on the glass **100**, a light emitting device **200-1** to **200-3** disposed on the TFT layer **3000'** and respectively included in a sub pixel of the display panel **1000'**, the various circuits **400** for driving the driving circuit **300**, and a connection cable **500** electrically connecting the TFT layer **3000'** with the various circuits **400**.

The TFT layer **3000'** may include a driving circuit **300** implemented as TFTs, and may be formed on a first surface of the glass **100**.

The various circuits **400** may include a MUX circuit for operation of the driving circuit **300**, an electro static discharge (ESD) circuit, a power circuit, a clock provision circuit, a gate driver, a data driver, and etc., and may be disposed or arranged on a second surface of the glass **100**.

According to an example embodiment, the display panel **1000'** may include the connection cable **500** disposed in an edge area of a TFT substrate, and electrically connecting the TFT layer **3000'** disposed on a first surface of the glass **100** with the various circuits **400** disposed on a second surface of the glass **100**.

The connection cable **500** is disposed in the edge area of the TFT substrate because otherwise, a crack may occur on the glass due to a difference of temperature between a fabrication process of a TFT substrate and a process of filling a hole with conductive materials, where a hole penetrating the glass **100** is disposed and circuits arranged on the opposite sides of the glass **100** are connected to each other,

In the example described above, all circuits for operation of the driving circuit **300** are, as in the reference numeral **400**, separately disposed on the opposite side of the glass **100** surface on which the TFT layer **3000'** is disposed. However, the example is not limited thereto. That is, all or some of the various circuits described above may be disposed on the TFT layer **3000'**.

For example, all the various circuits described above may be disposed on the TFT layer **3000'**. In this case, it is not necessary that a circuit is additionally arranged on the other surface of the glass **100** and accordingly, the connection cable **500** of FIG. **5** connecting front and rear surfaces of the glass **100** would not be necessary, either.

As another example, the MUX circuit, the ESD circuit, the power circuit, the clock provision circuit, and the gate driver may be implemented as TFTs and included in the TFT layer **3000'**, and the display panel may be implemented in such a way that the data driver circuit is additionally arranged on the other side of the glass **100**. FIG. **6** is a diagram provided to explain such an example embodiment.

FIG. **6** is a cross-sectional view of a TFT layer **3000'**, according to an example embodiment. In detail, FIG. **6** illustrates a disposition of various circuits included in the TFT layer **3000'** of the display panel **1000'**.

Referring to FIG. **6**, an entire pixel area **20** occupied by (or corresponding to) one pixel in the TFT layer **3000'** may include an area **10** in which various driving circuits **300** for driving the R, G and B sub pixels are arranged, and a peripheral remaining area **11**.

According to an example embodiment, a size of the area **10** occupied by a driving circuit **300** for the respective R, G and B sub pixels may be, for example, a size of about a quarter of the entire pixel area **20**, but is not limited thereto.

As described above, one pixel area **20** may include the remaining area **11** in addition to the area **10** occupied by the driving circuit **300** for driving the respective sub pixels, and so may the other pixels.

That is, according to an example embodiment, many spaces other than an area occupied with the driving circuit **300** are present in the TFT layer **3000'**, and thus, the ESD circuit **61**, the MUX circuit **62**, the power circuit **63**, the clock provision circuit **64**, and the gate driver circuit **65** may be implemented as TFTs and included in the remaining area **11** of the TFT layer **3000'** as illustrated in FIG. **6**. In this case, the data driver circuit may be arranged on the other surface of the glass **100** as in the reference numeral **400** of FIG. **5**.

Meanwhile, the location, size and number of the respective ESD circuit **61**, the MUX circuit **62**, the power circuit **63**, the clock provision circuit **64**, and the gate driver circuit **65** is only a non-limiting example.

In addition, an example embodiment in which various circuits are arranged on both sides as being divided based on the glass **100** is not limited to the example illustrated in FIG. **6**, and at least one circuit from among the ESD circuit **61**, the MUX circuit **62**, the power circuit **63**, the clock provision circuit **64**, and the gate driver circuit **65** of FIG. **6** may be arranged on the other surface of the glass **100** as in the reference numeral **400**.

A constitution and operation of the driving circuit **300** according to various example embodiments will be described in detail with reference to FIGS. **7**, **8**, **9**, **10**, **11**A and **11**B.

FIG. **7** is a block diagram related to one sub pixel, according to an example embodiment. That is, FIG. **7** illustrates only one light emitting device **200**, and a driving circuit **300** for driving the one light emitting device **200**. Accordingly, the light emitting device **200** and the driving circuit **300** as illustrated in FIG. **7** may be provided in the display panel **1000** and **1000'** by the sub pixel. Meanwhile, the light emitting device **200** may be a micro-LED in any one color from among R, G and B.

As described above, the driving circuit **300** may receive application of a PAM data voltage and a PWM data voltage, and control an amplitude and a pulse width of a driving current driving the light emitting device **200**. To this end, the driving circuit **300** may include a PAM driving circuit **310** and a PWM driving circuit **320** as illustrated in FIG. **7**.

The driving circuit **300** may be provided for each sub pixel, and one driving circuit **300** drives one sub pixel and thus may be referred to as a pixel circuit depending on circumstances. In this case, the PAM driving circuit **310** may be referred to as a PAM pixel circuit, and the PWM driving circuit **320** may be referred to as a PWM pixel circuit. For convenience of explanation, the terms "driving circuit" "PWM driving circuit" and "PWM driving circuit **320**" are used to describe an example embodiment.

Referring to FIG. **9**, the PAM driving circuit **310** may include a first driving transistor **311**, and control an amplitude of a driving current provided to the light emitting device **200** based on the applied PAM data voltage. The PWM driving circuit **320** may include a second driving transistor **321**, and control a pulse width of a driving current provided to the light emitting device **200** based on the applied PWM data voltage.

The first driving transistor **311** may provide a driving current of different amplitudes to the light emitting device **200** according to a magnitude of voltage applied to a gate terminal C. Accordingly, the PAM driving circuit **310** may provide a driving current having an amplitude corresponding to the applied PAM data voltage to the light emitting device **200** via the first driving transistor **311**.

The second driving transistor **321** may be connected to the gate terminal C of the first driving transistor **311**, and control a gate terminal voltage of the first driving transistor **311**, thereby controlling a pulse width of a driving current.

For example, after the light emitting device **200** starts light emission according to a driving current provided by the first driving transistor **311**, when a duration corresponding to a PWM data voltage has elapsed, the second driving transistor **321** may turn off the first driving transistor **311** and control a pulse width of the driving current.

Accordingly, the PWM driving circuit **320** may control a duration of a driving current (that is, a driving current having an amplitude corresponding to the PAM data voltage) provided to the light emitting device **200** by the PAM driving current on the basis of the PWM data voltage, and thereby a pulse width of the driving current can be controlled.

The light emitting device **200** may emit light according to a driving current provided by the driving circuit **300**. For example, the light emitting device **200** may emit light with different brightnesses according to an amplitude or a pulse width of a driving current provided from the driving circuit **300**. Here, the pulse width of the driving current may be expressed as a duty ratio of the driving current or a driving time of the driving current.

For example, the light emitting device **200** may emit light having a higher brightness with the increase in the amplitude of the driving current and with the increase in the pulse width (that is, with the increase in the duty ratio or with the increase in the driving time). However, the example is not limited thereto.

According to an example embodiment, the driving circuit **300** may compensate a deviation between driving circuits included in each of a plurality of sub pixels based on a driving voltage (VDD) driving the driving circuit **300**.

For example, a plurality of sub pixels are present in the display panel **1000** and **1000'**, and the respective sub pixels may include the corresponding first driving transistor **311**. Theoretically, a transistor fabricated under the same condition has the same threshold voltage. However, actual transistors may have different threshold voltages even if they are fabricated under the same condition, and so may the first driving transistors **311** included in the display panel **1000** and **1000'**.

As described above, in a case that the first driving transistors **311** corresponding to the respective sub pixels have different threshold voltages, the first driving transistors **311** may apply a driving current of different amplitudes corresponding to a difference of threshold voltages to the respective light emitting devices **200** even if the same PAM data voltage is applied to the gate terminal, and this may be displayed as a stain on the image and the like. Accordingly, it is necessary to compensate a deviation of threshold voltage between the first driving transistors **311** included in the display panel **1000** and **1000'**.

Meanwhile, a deviation of threshold voltage is present in the second driving transistors **321** present for each sub pixel of the display panel **1000** and **1000'**, and if the deviation is not compensated, even if the same PWM data voltage is applied to the second driving transistors **321**, a driving current of different pulse widths corresponding to the deviation of threshold voltage is provided to the respective light emitting device **200**, which is a problem. This is described with regard to the PAM driving circuit **310** above. Accordingly, it is necessary to compensate a deviation of threshold voltage between the second driving transistors **321** included in the display panel **1000** and **1000'** as well.

The deviation between the driving circuits described above may be a deviation of threshold voltage between the first driving circuits and a deviation of threshold voltage between the second driving circuits respectively corresponding to a plurality of sub pixels of the display panel **1000**.

For example, when the driving voltage (VDD) is applied, the PAM driving circuit **310** may apply, to a gate terminal C of the first driving transistor **311**, a voltage (hereinafter referred to as "first voltage") based on the driving voltage (VDD) and the threshold voltage of the first driving transistor **311**. Accordingly, the first driving transistor **311** may, regardless of the threshold voltage of the first driving transistor **311**, provide, to the light emitting device **200**, a driving current having an amplitude corresponding to a magnitude of a PAM data voltage to be applied later.

When the driving voltage (VDD) is applied, the PWM driving circuit **320** may apply, to a gate terminal A of the second driving transistor **321**, a voltage (hereinafter referred to as "second voltage") based on the driving voltage (VDD) and the threshold voltage of the second driving transistor **321**. Accordingly, the first driving transistor **321** may, regardless of the threshold voltage of the first driving transistor **321**, provide, to the light emitting device **200**, a driving current having a pulse width corresponding to a magnitude corresponding to a PAM data voltage to be applied later.

Accordingly, it is possible to solve a problem caused by a deviation between driving circuits included in the display panel **1000** and **1000'**.

According to an example embodiment, when after a first voltage is applied to the gate terminal C of the first driving transistor **311** and a second voltage is applied to the gate terminal A of the second driving transistor **321** as described above, when a PAM data voltage and a PWM data voltage are applied, the driving circuit **300** may provide, to the light emitting device **200**, a driving current of amplitude corresponding to the applied PAM data voltage and of a pulse width corresponding to the applied PWM data voltage.

For example, in a state that the first voltage is applied to the gate terminal C of the first driving transistor **311**, when the PAM data voltage is applied, the PAM driving circuit **310** may apply a voltage (hereinafter referred to as "third voltage") based on the first voltage and the applied PAM data voltage to the gate terminal C of the first driving transistor **311**.

In addition, in a state that the second voltage is applied to the gate terminal A of the second driving transistor **321**, when the PWM data voltage is applied, the PWM driving circuit **320** may apply a voltage (hereinafter referred to as "fourth voltage") based on the second voltage and the applied PWM data voltage to the gate terminal A of the second driving transistor **321**.

Accordingly, in a state that the third voltage is applied to the gate terminal C of the first driving transistor **311** and the fourth voltage is applied to the gate terminal A of the second driving transistor **321**, when a driving voltage (VDD) is applied to the light emitting device **200**, the PAM driving circuit **310** may provide a driving current source of an amplitude corresponding to the PAM driving voltage to the light emitting device **200**, and the light emitting device **200** starts emitting light.

In this case, a sweep signal (linear shift voltage) may be applied to the PWM driving circuit **320**, and the second driving transistor **321** in an off state may remain in the off state until a voltage of the gate terminal A is linearly shifted from the fourth voltage to the second voltage according to the sweep signal.

When the voltage of the gate terminal A of the second driving transistor **321** reaches the second voltage, the second driving transistor **321** may be turned on, and the driving voltage (VDD) applied to the source terminal of the second driving transistor **321** may be accordingly applied to the gate terminal C of the first driving transistor **311** via the drain terminal.

The driving voltage (VDD) is applied to the source terminal of the first driving transistor **311**. Thus, when the driving voltage (VDD) is applied to the gate terminal C of the first driving transistor **311**, a voltage between the gate terminal and the source terminal of the first driving transistor **311** may exceed the threshold voltage of the first driving transistor **311** and the first driving transistor **311** may be turned off. For reference, a threshold voltage of a PMOSFET has a negative value. When a voltage less than or equal to the threshold voltage is applied to in between a gate terminal and a source terminal of the PMOSFET, the PMOSFET is turned off. When a voltage greater than the threshold voltage is applied, the PMOSFET is turned off. When the first driving transistor **311** is turned off, the driving current may no longer flow, and the light emitting device **200** stops light emission.

As described above, the PWM driving circuit **320** may control the voltage of the gate terminal A of the first driving transistor **311** and control a pulse width of the driving current.

The following will explain the operation regarding a threshold voltage compensation of the second driving transistor **321** in detail by referring to FIG. **8**. FIG. **8** is a circuit diagram of a pulse width modulation (PWM) driving circuit **320**, according to an example embodiment. Numerical values of the various voltages described below are only an example, and the example is not limited to the corresponding values.

Referring to FIG. **8**, the PWM driving circuit **320** may include a third transistor **322** connected to and disposed between a drain terminal and a gate terminal of the second driving transistor **321**, a fourth transistor **323** including a drain terminal commonly connected to the gate terminal A of the second driving transistor **321** and the source terminal of the third transistor **322**, a third capacitor **324** including a first terminal commonly connected to the gate terminal A of the second driving transistor **321**, the source terminal of the third transistor **322** and the drain terminal of the fourth transistor **323**, a fifth transistor **325** including a source terminal via which a PWM data voltage is applied, and a drain terminal connected to a second terminal B of the third capacitor **324**, and a fourth capacitor **326** including a first terminal commonly connected to a second terminal of the third capacitor **324** and the drain terminal of the fifth transistor **325**, and a second terminal receiving a linearly-shifting sweep signal.

As described above, when the driving voltage (VDD) is applied to the PWM driving circuit **320**, the PWM driving circuit **320** may apply a voltage corresponding to the sum of the driving voltage (VDD) and a threshold voltage of the second driving transistor **321**, that is, the second voltage, to the gate terminal A of the second driving transistor **321**, and compensate the threshold voltage of the second driving transistor **321**.

First, the PWM driving circuit **320** may initialize each of the node B and the node A. For example, the PWM driving circuit **320** may receive input of an initial voltage (for example, −5V) from a data line (Sig<m>) via the fifth transistor **325** turned on according to a control signal SPWM (n) and apply the received initial voltage input to the node B, and receive input of an input voltage (for example, −5V) from the data line (Sig<m>) via the fourth transistor **323** turned on according to a control signal Ref and apply the received initial voltage input to the node A.

Then, the driving voltage (VDD) (for example, +8V) may be input to the source terminal of the second driving transistor **321** via a driving voltage terminal. In this case, the third transistor **322** is in a turn-on state according to a control signal RES, and the second driving transistor **321** has a gate terminal A voltage of −5V which is a low state, and thus may be fully turned on.

Accordingly, the input driving voltage (VDD) is applied to the gate terminal A of the second driving transistor **321** while sequentially going through the second driving transistor **321** and the third transistor **322**. However, in this case, the voltage of the gate terminal A of the second driving transistor **321** may rise up to only a voltage corresponding to the sum of the driving voltage and the threshold voltage of the second driving transistor **321** rather than rising up to the input driving voltage (VDD).

When the driving voltage (VDD) is first applied via the source terminal of the second driving transistor **321**, a voltage of the gate terminal A of the second driving transistor **321** is in a low state (for example, −5V) and the second driving transistor **321** is fully turned on, and thus a sufficient current flows and the gate terminal A voltage of the second driving transistor **321** smoothly rises. However, a difference of voltage between the gate terminal and the source terminal of the second driving transistor **321** is reduced with the increase of the gate terminal A voltage of the second driving transistor **321**, and thus a current flow decreases, and as a result, when the difference of voltage between the gate terminal and source terminal of the second driving transistor **321** reaches the threshold voltage of the second driving transistor **321**, the second driving transistor **321** is turned off and the current flow is stopped.

That is, the driving voltage (VDD) is applied to the source terminal of the second driving transistor **321**, and thus the voltage of the gate terminal A of the second driving transistor **321** may rise only up to a voltage (that is, the second voltage) corresponding to the sum of the driving voltage (VDD) and the threshold voltage of the second driving transistor **321**. As described above, the second voltage is applied to the gate terminal A of the second driving transistor **321**, thereby compensating the threshold voltage of the second driving transistor **321**.

Meanwhile, the structure and operation of the PAM driving circuit **310** regarding compensation of threshold voltage of the first driving transistor **311** are similar to the description regarding compensation of threshold voltage of the second driving transistor **321** described above. Thus, the structure and operation of the PAM driving circuit **310** regarding compensation of threshold voltage of the first driving transistor **311** would have been easily understood through the circuit diagram illustrated in FIG. **9** and the timing diagram of FIG. **10**, and thus the overlapping description will be omitted herein.

As described above, according to an example embodiment, a threshold voltage of the second driving transistor **321** included in the respective sub pixels of the display panel **1000** and **1000'** may be internally compensated, and so may a threshold voltage of the first driving transistor **311**.

Here, the term "internal compensation" means that threshold voltages of the first and second driving transistors **311** and **321** are autonomously compensated within the driving circuit **300** while the driving circuit **300** is operated due to a connection structure of the devices as illustrated in FIG. **8**, and this internal compensation method is distinct from an external compensation method to compensate threshold voltages of the first and second driving transistors **311** and **321** by correcting a data voltage itself to be applied from outside of the driving circuit **300** to the driving circuit **300**.

As described above, according to an example embodiment, the threshold voltages of the driving transistors **311** and **321** included in the display panel **1000** and **1000'** are internally compensated and thus, when applying or setting a PAM data voltage to all pixels (or all sub pixels) of the display panel **1000** and **1000'** to display one image frame, the PAM data voltage may be applied at once to all the pixels (or all the sub pixels) included in the display panel **1000** and **1000'**. Accordingly, it is possible to secure a sufficient light emitting interval for the light emitting device **200** to emit light from among the entire time interval for displaying one image frame.

This is a distinct feature from an external compensation method in which it is necessary to sequentially scan the pixels included in the display panel **1000** and **1000'** for each line and separately apply the PAM data voltage for which the threshold voltage has been compensated for each line.

According to the example embodiment described above, the PWM data voltage may be sequentially applied to the pixels included in the display panel **1000** and **1000'** for each line to express a grayscale or gradation for each line.

The following will explain the details and operation of the driving circuit **300** in detail by referring to FIGS. **9** and **10**.

FIG. **9** is a detailed circuit diagram of a driving circuit **300**, according to an example embodiment. The devices included in the driving circuit **300** and a connection relationship between the devices will be first described with reference to FIG. **9**.

FIG. **9** illustrates one sub pixel-related circuit, that is, one light emitting device **200**, and a driving circuit **300** for driving the light emitting device **200**. Accordingly, the light emitting device **200** and the driving circuit **300** as illustrated in FIGS. **7**A and **7**B may be provided in the display panel **1000** and **1000'** by the sub pixel. Meanwhile, the light emitting device **200** may be an LED in any one color from among R, G and B.

Referring to FIG. **9**, the driving circuit **300** may include a PAM driving circuit **310**, a PWM driving circuit **320**, sixth to eighth transistors **331**, **332** and **361**.

The PAM driving circuit **310** may include a first transistor **312** which is connected to and disposed between the drain terminal and the gate terminal of the first driving transistor **311**, a first capacitor **313** including a first terminal commonly connected to the source terminal of the first driving transistor **311**, the source terminal of the second driving transistor **321** and the driving voltage (VDD) terminal of the driving circuit **300**, a second capacitor **314** including a first terminal commonly connected to the gate terminal C of the first driving transistor **311**, a second terminal of the first capacitor **313** and the source terminal of the first transistor **312**, and a second transistor **315** including a source terminal via which a data signal (Sig<m>) is applied, and a drain terminal connected to the second terminal D of the second capacitor **314**.

While the first transistor **312** is turned on according to a control signal RES, when the driving voltage (VDD) is applied to the PAM driving circuit **310** by the driving voltage (VDD) terminal via the source terminal of the first driving transistor **311**, the PAM driving circuit **310** may apply a first voltage corresponding to the driving voltage (VDD) and the threshold voltage of the first driving transistor **311** to the gate terminal C of the first driving transistor **311** via the turned-on driving transistor **311**.

In addition, when the PAM data voltage is applied via the source terminal of the second transistor **315**, the PAM driving circuit **310** may apply a third voltage corresponding to the sum of the first voltage and the applied PAM data voltage to the gate terminal C of the first driving transistor **311**. A voltage corresponding to the sum of the applied PAM data voltage and the threshold voltage of the first driving transistor **311** may be charged in the opposite terminals of the first capacitor **313**.

The PWM driving circuit **320** may, as described above, include the third transistor **322** connected to and disposed between the drain terminal and the gate terminal of the second driving transistor **321**, the fourth transistor **323** including a drain terminal commonly connected to the gate terminal A of the second driving transistor **321** and the source terminal of the third transistor **322**, the third capacitor **324** including a first terminal commonly connected to the gate terminal A of the second driving transistor **321**, the source terminal of the third transistor **322** and the drain terminal of the fourth transistor **323**, the fifth transistor **325** including a source terminal via which a data voltage (Sig<m>) is applied, and a drain terminal connected to the second terminal B of the third capacitor **324**, and the fourth capacitor **326** including a first terminal commonly connected to a second terminal of the third capacitor **324** and the drain terminal of the fifth transistor **325**, and a second terminal receiving a linearly-shifting sweep signal.

While the third transistor **322** is turned on, when the driving voltage (VDD) is applied to the PWM driving circuit **320** by the driving voltage terminal via the source terminal of the second driving transistor **321**, the PWM driving circuit **320** may apply a second voltage corresponding to the driving voltage (VDD) and the threshold voltage of the second driving transistor **321** to the gate terminal A of the second driving transistor **321** via the turned-on driving transistor **321**.

In addition, when the PWM data voltage is applied to the PWM driving circuit **320** via the source terminal of the fifth transistor **325**, the PWM driving circuit **320** may apply a fourth voltage corresponding to the sum of the second voltage and the applied PWM data voltage to the gate terminal of the second transistor **321**.

The sixth transistor **331** may include a source terminal which is commonly connected to the drain terminal of the second driving transistor **321** and the drain terminal of the third transistor **322**, and a drain terminal which is commonly connected to the gate terminal C of the first driving transistor **311**, the second terminal of the first capacitor **313**, the first terminal of the second capacitor **314**, and the source terminal of the first transistor **312**. The sixth transistor **331** may be turned on or off according to the control signal Emi, and electrically connect the PAM driving circuit **310** and the PWM driving circuit **320** or separate them from each other.

The seventh transistor **332** may include a source terminal commonly connected to the drain terminal of the first driving transistor **311** and the drain terminal of the first transistor **312**, and a drain terminal connected to an anode terminal of the light emitting device **200**. The seventh transistor **332** may be turned on or off according to the control signal Emi, and electrically connect the PAM driving circuit **310** and the light emitting device **200** or separate them from each other.

The eighth transistor **361** may be connected to and disposed between the anode terminal and cathode terminal of the light emitting device **200**. Before the light emitting device **200** is mounted on the TFT layer **3000** and electrically connected to the driving circuit **300**, the eighth transistor **361** may be turned on according to the control signal Test to check the abnormality of the driving circuit **300**, and after the light emitting device **200** is mounted on the TFT layer **3000** and electrically connected to the driving circuit **300**, the eighth transistor **361** may be turned on according to a control signal (Discharging) to discharge the charge remaining in the light emitting device **200**.

Meanwhile, the cathode terminal of the light emitting device **200** may be connected to a ground voltage (VSS) terminal.

The following will explain the operation of the driving circuit **300** in detail by referring to FIG. **10**. FIG. **10** is a timing diagram of various signals for driving a driving circuit of FIG. **9**, according to an example embodiment. Numerical values of the various voltages and times described below are only an example, and the example is not limited to the corresponding values. In addition, the name of the respective durations is not limited to the illustration of FIG. **10**.

Referring to FIG. **10**, the driving circuit **300** may be, to display one image frame, driven in the order of a node initialization duration (Initialize), a threshold voltage (Vth) compensation duration, a data voltage setup duration, a light emitting duration (Emitting), and a discharge duration (LED Discharging).

The initialization duration may include an initialization duration of nodes B and D and an initialization duration of nodes A and C.

The initialization duration is a duration for initializing voltages of the second terminal of the third capacitor **324** (that is, the node B) and the second terminal of the second capacitor **315** (that is, the node D) to stabilize voltages of the second and first driving transistors **321** and **311** (that is, the node A and the node B).

The driving circuit **300** may initialize the voltages of the B and D terminals to the initial voltage (for example, −5V) during the initialization duration of the nodes B and D. For example, the fifth transistor **325** and the second transistor **315** are turned on according to the control signals SPWM(n) and SPAM during the initialization duration of the nodes B and D, and thus an initial voltage (for example, −5V) applied by the data signal line (Sig<m>) may be applied to the node B via the fifth transistor **325**, and applied to the node B via the second transistor **315**.

The initialization duration of nodes A and C is a duration for initializing voltages of the gate terminal of the second driving transistor **321** (that is, the node A) and the gate terminal of the first driving transistor **311** (that is, the node C).

During the initialization duration of nodes A and C, the control signals RES, Ref and Emi as well as the control signals SPWM(n) and SPAM have a low voltage (for example, −5V). In addition, a low voltage (for example,

−5V) may be applied to the driving voltage (VDD) terminal and the ground voltage (VSS).

Accordingly, the initial voltage (for example, −5V) applied by the data signal line (Sig<m>) may be applied to the node A via the fourth transistor **323** turned on according to the control signal Ref, and applied to the node C via the third transistor **322** turned on according to the control signal RES and the sixth transistor **331** turned on according to the control signal Emi.

The initial voltage (for example, −5V) is applied to the anode terminal of the light emitting device **200** via the first transistor **312** turned on according to the control signal RES and the seventh transistor **332** turned on according to the control signal Emi, and thus −5V may be applied to each of the opposite terminals of the light emitting device **200** and the light emitting device **200** may not emit light.

Meanwhile, during the initialization duration of the nodes A and C, a voltage of the driving voltage (VDD) terminal rises from a low voltage (−5V) to the driving voltage (VDD, for example, +8V) because it is necessary to apply the driving voltage (VDD) to the driving voltage (VDD) terminal to enable the light emitting device **200** to emit light.

A voltage of the driving voltage terminal is raised immediately after the nodes A and C are initialized as illustrated in FIG. **10** rather than during the data voltage setup/threshold voltage (Vth) compensation duration or light emitting duration (Emitting) because it is more stable to perform the following operations after an effect from a voltage shift of the driving voltage terminal being coupled to the respective nodes of the driving circuit **300** is stabilized.

Meanwhile, the voltages of the nodes A and C are initialized as described above to maintain the first and second driving transistors **311** and **321** in a turn-on state when the threshold voltages of the first and second driving transistors **311** and **321** are compensated.

For example, for a threshold voltage compensation, it is necessary that the first and second driving transistors **311** and **321** are in a turn-on state. However, according to an example embodiment, the initial voltage is applied to the nodes A and C at the time of threshold voltage compensation, and thus, even if the driving voltage (VDD) is coupled and the voltages of the nodes A and C are raised to a certain extent as described above, the first and second driving transistors **311** and **321** may remain in the turn-on state. Accordingly, according to an example embodiment, the initial voltage may be appropriately set in relation to the driving voltage (VDD).

The threshold voltage compensation duration is a duration for compensating the threshold voltages (Vth) of the first and second driving transistors **311** and **321**. During the threshold voltage compensation duration, both sixth and seventh threshold transistors **331** and **332** are turned off according to the control signal Emi, and thus the threshold voltage compensation may be carried out in the PAM driving circuit **310** and the PWM driving circuit **320** which are independent of each other.

For example, during the threshold voltage compensation duration, the control signal RES remains in a low state, and thus the first and third transistors **312** and **322** may remain in a turn-on state. In addition, as described above with reference to the initialization duration, the first and second driving transistors **311** and **312** may be in a turn-on state as well.

Accordingly, when the voltage of the driving voltage terminal rises from the low voltage (−5V) to the driving voltage (VDD, +8V), the driving voltage (VDD) may be applied to the node A through the second driving transistor **321** and the third transistor **322** in a sequence and the threshold voltage compensation of the second driving transistor **321** may be initiated. Accordingly, when the voltage of the node A becomes the second voltage, the second driving transistor **321** may be turned off and the compensation of threshold voltage of the second driving transistor **321** may be ended.

When the voltage of the driving voltage terminal rises from the low voltage (−5V) to the driving voltage (VDD, +8V), the driving voltage (VDD) may be applied to the node C as well through the first driving transistor **311** and the first transistor **312** in a sequence. Accordingly, the threshold voltage compensation of the first driving transistor **311** may be initiated, and when the first voltage is applied to the voltage of the node C, the first driving transistor **311** may be turned off and the compensation of threshold voltage of the first driving transistor **311** may be ended.

When the compensation is ended, the nodes A and C may remain in a floating state.

The data voltage setup duration is a duration for respectively setting a data voltage to the PAM driving circuit **310** and the PWM driving circuit **320**.

According to an example embodiment, as illustrated in FIG. **10**, the PWM data voltage setup may be performed first and then, the PAM data voltage setup may be performed. However, in an implementation, the order may be changed.

During the data voltage setup duration, both sixth and seventh transistors **331** and **332** are in a turn-off state according to the control signal Emi, and thus a data voltage may be set to the PAM driving circuit **310** and the PWM driving circuit **320** which are independent of each other.

First, the PWM data voltage setup duration (PWM data+Vth compensation) is a duration for which the PWM data voltage transferred from the data line (Sig<m> cable) is applied to the gate terminal (node A) of the second driving transistor **321**. For example, when the fifth transistor **325** is turned on according to the control signal SPWM(n) (for example, −5V), the PWM data voltage applied via the source terminal of the fifth transistor **325** may be applied to the node A via the fifth transistor **325** and the third capacitor **324**. Accordingly, a fourth voltage corresponding to the sum of the second voltage and the PWM data voltage may be input to the node A.

Meanwhile, the control signal SPWM(n) may be a signal which is output from a gate driver inside or outside of the display panel **1000** and **1000'**. In the SPWM(n)), the n refers to a number of pixel lines included in the display panel **1000** and **1000'**.

For example, in a case that a plurality of pixels arranged in a matrix form in the display panel **1000** and **1000'** constitute 270 horizontal lines (or rows), a gate driver may output a control signal, that is, SPWM **1** to SPWM **270**, that sequentially turns on, for each line, the fifth transistor **325** of pixels (or sub pixels) included in the respective lines from line **1** to line **270**.

Accordingly, the fifth transistor **325** of the pixels (or sub pixels) included in the display panel **1000** and **1000'** may be sequentially turned on for each line, and the PWM data voltage may be sequentially applied to a plurality of pixels arranged in the matrix form (that is, a plurality of PWM driving circuits **320**) for each line of the plurality of pixels.

First, the PAM data voltage setup duration (PWM data+Vth compensation) is a duration for which the PAM data voltage transferred from the data line (Sig<m> cable) is applied to the gate terminal (node C) of the first driving transistor **311**. For example, when the second transistor **315** is turned on according to the control signal SPAM (for example, −5V), the PAM data voltage applied via the source terminal of the second transistor **315** may be applied to the node C via the second transistor **315** and the second capacitor **314**. Accordingly, a third voltage corresponding to the sum of the first voltage and the PAM data voltage may be input to the node C.

Meanwhile, the control signal SPAM may be a signal which is output from a gate driver inside or outside of the display panel **1000** and **1000'**. According to an example embodiment, the control signal SPAM may be, unlike the control signal SPWM(n), applied at once to all pixels (or all sub pixels) included in the display panel **1000** and **1000'**.

For example, in a case that a plurality of pixels arranged in a matrix form in the display panel **1000** and **1000'** constitute 270 horizontal lines (or rows), a gate driver may output a control signal, that is, a SPAM, that turns on the second transistor **315** of all pixels (or sub pixels) included in the 270 horizontal lines (or rows) included in the display panel **1000** and **1000'** at once.

Accordingly, the second transistor **315** of all pixels (or sub pixels) included in the display panel **1000** and **1000'** may be turned on at once, and the PAM data voltage may be applied at once to a plurality of pixels arranged in the matrix form (that is, a plurality of PAM driving circuits **320**).

According to an example embodiment, the PAM data voltage applied at once to all sub pixels (more accurately, all PAM driving circuits **310**) included in the display panel **1000** and **1000'** may be a voltage of the same magnitude.

In addition, according to an example embodiment, the display panel **1000** and **1000'** may be divided into a plurality of areas, wherein the PAM data voltage applied at once to all sub pixels (more accurately, all PAM driving circuits **310**) included in the display panel **1000** and **1000'** may be applied differently according to areas. This will be explained in more detail hereinbelow with reference to FIGS. **12**A and **12**B.

The light emitting duration (Emitting) is a duration for which the light emitting device **200** emits light. During the light emitting duration, the light emitting device **200** may emit light according to an amplitude and a pulse width of a driving current provided by the driving circuit **300**, thereby expressing a grayscale or gradation corresponding to the applied PAM data voltage and the applied PWM data voltage.

For example, during the light emitting duration, the sixth to seventh transistors **331** to **332** are turned on according to the control signal Emi, and thus the PAM driving circuit **310**, the PWM driving circuit **320** and the light emitting device **200** may be electrically connected to each other.

When the light emitting duration is initiated, the driving voltage (VDD, for example, +8V) may be transferred to the light emitting device **200** via the first driving transistor **311** and the seventh transistor **332**, and thus a potential difference of +13 V may occur at both terminals of the light emitting device **200** and the light emitting device **200** may emit light. The driving current illuminating the light emitting device **200** may have an amplitude corresponding to the PAM data voltage.

During the light emitting duration, a sweep voltage (Vsweep) which is a linearly-shifting voltage may be applied to the fourth capacitor **326**. For example, in a case that the sweep voltage (Vsweep) is a voltage gradually decreased from +6V to 0V, the sweep voltage may be transferred to the gate terminal (that is, the node A) of the second driving transistor **321** in a floating state via the fourth capacitor **326** and the third capacitor **324**.

Accordingly, the voltage of the node A is reduced from the fourth voltage according to the sweep voltage, and when the decreasing voltage of the node A becomes the second voltage, the second driving transistor **321** changes from a turn-off state to a turn-on state. For example, during the light emitting duration, the driving voltage (VDD) is applied to the source terminal of the second driving transistor **321**, and thus, when a voltage less than or equal to the second voltage (that is, a voltage corresponding to the sum of the driving voltage (VDD) and the threshold voltage of the second driving transistor **321**) is applied to the node A, a voltage between a gate and source of the second driving transistor **321** may be lower than the threshold voltage and the second driving transistor **321** may be thereby turned on.

When the second driving transistor **321** is turned on, the driving voltage (VDD) may be transferred to the node C via the sixth transistor **331**. When the driving voltage (VDD) is transferred to the node C, a voltage between the gate and the source of the first driving transistor **311** may become 0V which is greater than or equal to the threshold voltage of the first driving transistor **311**, and thus the first driving transistor **311** may be turned off. When the first driving transistor **311** is turned off, the driving voltage (VDD) may not reach the light emitting device **200** and thus, the light emission of the light emitting device **200** may be ended.

As described above, from a time when the driving voltage (VDD) (for example, +8V) is applied to the light emitting device **200** until a time when a voltage applied to the gate terminal A of the second driving transistor **321** is shifted according to the sweep voltage (Vsweep) and becomes the second voltage, the PWM driving circuit **320** may provide the driving current to the light emitting device **200**. That is, the driving current may have a pulse width of a magnitude corresponding to the PWM data.

Meanwhile, an electrical charge remaining in the light emitting device **200** may be present even when the light emission of the light emitting device **200** has ended. Accordingly, a problem that the light emitting device **200** is slightly illuminated after the light emission has ended may be caused, which may be a problem especially when a low grayscale or gradation (for example, black) is expressed.

The discharge duration (LED discharging) is an interval for discharging an electrical charge remaining in the light emitting device **200** after the light emitting duration ends. The driving circuit **300** may turn on the eighth transistor **361** according to the control signal (Discharging) so that the electrical charge remaining in the light emitting device **200** is fully discharged to the ground voltage (VSS) and accordingly, the problem mentioned above can be solved.

Meanwhile, before the light emitting device **200** is mounted on the TFT layer **3000** and electrically connected to the driving circuit **300**, the eighth transistor **361** may be used to check the abnormality of the driving circuit **300**. For example, the engineer or manufacturer of the product may, like the control signal Test, turn on the eighth transistor **361** during the light emitting duration and then identify a current flowing through the eighth transistor **361**, and thereby the abnormality (for example, a short or open of a circuit, etc.) of the driving circuit **300** may be checked.

The various data signal (Sig<m>), the power signal (VDD and VSS) and the control signal (RES, Ref, SPWM(N), SPAM, Emi, Vsweep, Test, and Discharging) illustrated in FIG. **10** may be received from an external timing controller (TCON), a processor, various drivers (for example, data driver and gate driver), etc. This feature is not related to the main idea of one or more example embodiments and thus a detailed description thereof is omitted herein.

As illustrated in FIG. **10**, according to an example embodiment, the PAM data voltage may be applied at once to all PAM driving circuits **310** included in the display panel **1000** and **1000'**. In this way, a threshold voltage of a driving transistor of a PAM driving circuit is compensated in an external compensation way, which is different from a related art where it is necessary to scan a pixel line to set a PAM data voltage.

For example, in a case that an image is displayed at 120 Hertz (Hz), it takes 8300 microseconds (μs) to display one image frame. However, in a case that a display panel includes 270 horizontal lines (rows), it takes a time of approximately 2470 μs to scan all the lines.

Accordingly, in a case that an external compensation method is used, to set a PWM data voltage and a PAM data voltage to the entire driving circuits included in the display panel, it takes approximately 5000 μs, and thus, it is unlikely that a percentage of time that may be occupied by a light emitting duration per frame will exceed 40%, as shown in (3300/8300)*100=39.8%.

However, according to an example embodiment, the PAM data voltage is applied at once and set to the driving circuit **300**, and thus, when calculating a percentage of time that may be occupied by a light emitting duration per frame with reference to a time allocated to the respective durations illustrated in FIG. **10**, it may be understood that at least 65% is secured as shown in (5760/8300)*100=69.2%.

As described above, when a sufficient light emitting duration is secured, it is possible to delete various resources (for example, functions related to TCON, memory, data driver, PCT, etc.) required to externally compensate all threshold voltages of related-art PWM and PAM driving transistors, thus simplifying operations and reducing costs.

The shorter the light emitting duration, the shorter a light emission control duration for each grayscale or gradation. Thus, it may be difficult to express various grayscales or gradations through the PWM method. However, the example embodiment described above may solve this problem and may solve a problem for life extension of the light emitting device.

FIGS. **11**A and **11**B are experiment waveforms for nodes A and C of a driving circuit **300**, according to an example embodiment. In particular, FIG. **11**B is an enlarged view of 0 to 200 μs in the waveform illustrated in FIG. **11**A.

In the experiment, the driving voltage (VDD) is set to +8V, and both threshold voltages of the first and second driving transistors **311** and **321** are set to −4V.

According to an example embodiment, the PAM data voltage is, as illustrated in FIG. **10**, after the initialization duration of nodes B and D (20 μs), the initialization duration of nodes A and C (20 μs), the Vth compensation duration (20 μs) and the PWM data voltage setup duration (2470 μs); however, the PAM data voltage is applied at 2 ms for convenience of experiment. In addition, in FIG. **10**, an example in which the initialization duration of B and D nodes is 20 μs is described, but in the experiment of FIG. **11**B, it is set to 40 μs.

Referring to FIG. **11**B, it may be understood that the nodes B, D, A and D are initialized to −5V in the interval ① (the initialization duration of nodes B and D, 40 μs) and the interval ② (the initialization duration of nodes A and C, 40 μs to 60 μs).

In the middle of the interval ②, a voltage of a driving voltage terminal rises from −5V to +8V, and thus, it may be understood that due to a coupling effect, voltages of the nodes A and C rise up to approximately +2V. However, as described above, during the threshold voltage compensation duration, the driving voltage (+8V) is applied to the source terminals of the first and second driving transistors **311** and **321**, and thus a voltage between the gate and the source of the first and second driving transistors **311** and **321** may be less than or equal to the threshold voltage and the first and second driving transistors **311** and **321** may remain in a turn-on state.

Meanwhile, it may be understood that the voltages of the nodes A and C in the interval ③ (threshold voltage compensation duration) are approximately +4V, respectively. The driving voltage (VDD) is +8V and the threshold voltage of each of the first and second driving transistors **311** and **321** is −4V, and thus, it is necessary to apply +4V (the second voltage **72** and the first voltage **71**) corresponding to the sum of the two voltages to the respective nodes A and C, which matches with the experiment result illustrated in FIG. **11**B.

Then, when the PWM data voltage is applied at the time point ④, the voltage of the node A may rise up to the applied PWM data voltage and become a fourth voltage. When the PAM data voltage is applied at the time point ⑤ of FIG. **11**A, the voltage of the node C may rise up to the applied PAM data voltage and become a third voltage.

As described above, the respective data voltages may be set to the nodes A and C, and then the light emitting device **200** may emit light during the light emitting duration. In this case, the light emitting device **200** emits light for a time corresponding to the PWM data voltage, where the time corresponding to the PWM data voltage is a period from a time when the light emitting duration is started that is, when a driving voltage (VDD) is applied to the light emitting device **200**, to a time when a voltage applied to the node A is shifted according to the sweep signal (Vsweep) and becomes the second voltage.

Referring to FIG. **11**A, it may be understood that the light emitting device **200** emits light from a time when the light emitting duration **80** is started. In addition, it may be understood that a voltage of the node A is linearly reduced according to the sweep signal (Vsweep), and that when the linearly-reduced voltage of the node A reaches a particular voltage, the light emitting device **200** stops emitting light. (See, LED emission of FIG. **11**A)

FIGS. **12**A and **12**B are diagrams illustrating a high dynamic range (HDR) realized through a display panel **1000** and **1000'**, according to an example embodiment.

The HDR is a technology for further brightening an area with a brighter grayscale or gradation and darkening an area with a darker grayscale or gradation in a digital image to extend a dynamic range of brightness so that the digital image is visible as if the image is seen through naked eyes. The HDR function may be realized by means of the display panel **1000** and **1000'** according to the example embodiments.

According to an example embodiment, one large-scale display panel **10000** may be configured by combining a plurality of display panels **1000** and **1000'**. When it is assumed that the respective display panels **1000** and **1000'** included in the large-scale display panel **1000** is a modular panel, FIG. **12**A illustrates an example embodiment in which nine modular panels constitute one large-scale display panel **10000**. The number of modular panels included in the large-scale display panel **10000** is not limited thereto. For example, a large-scale display panel may be configured with various numbers of modular panels such as four, twelve, and the like.

As described above, the PAM data voltage applied at once to all sub pixels (more accurately, all PAM driving circuits **310**) included in the display panel **1000** and **1000'** may be a voltage of the same magnitude, and FIG. **9** corresponds to this example embodiment. That is, in the example of FIG. **9**, the PAM data voltage is applied at once to all sub pixels included in the display panel **1000** and **1000'** via one data line (Sig cable), and thus a PAM data voltage of the same magnitude may be applied. That is, the same PAM data voltage may be applied to one modular panel.

However, an example where it is necessary to apply the same PAM data voltage to all sub pixels is only limited to one display panel **1000** and **1000'**, and the respective modular panel further includes its own data line (Sig cable), and thus a PAM data voltage of different magnitudes may be applied for each modular panel.

Accordingly, in a case that a modular panel for which an HDR driving is required in the large-scale display panel **10000** as illustrated in FIG. **12**A, a PAM data voltage distinct from a PAM data voltage of another modular panel may be applied to the corresponding modular panel so that the HDR function is realized. For example, to express a brighter part of the image even brighter, a higher PAM data voltage than the other modular panel may be applied to a modular panel including the bright part.

Meanwhile, the example of implementation of the HDR function is not limited thereto. For example, as illustrated above, the display panel **1000** and **1000'**, that is, a modular panel may be divided into a plurality of areas and an HDR may be implemented by the plurality of areas.

The right drawing of FIG. **12**B illustrates an example embodiment in which one modular panel is divided into nine areas, that is, nine HDR blocks. However, example embodiments are not limited to any specific examples. For example, according to an example embodiment, one modular panel may be implemented to include various numbers of HDR blocks such as four, twelve, and the like.

In this case, it is necessary that a different PAM data voltage is applied to a block for which the HDR driving is required while applying a PAM data voltage at once to all sub pixels included in the modular panel. To this end, according to an example embodiment, an additional cable for applying the PAM data voltage for each HDR block may be provided.

The circuit diagram illustrated on the left side of FIG. **12**B illustrates a driving circuit **300** included in one sub pixel from among all sub pixels included in the HDR block **5**. As illustrated, it may be understood that an additional data line (PAM data (Block **5**), **90**) is included.

As described above, in a case that one display panel **1000** and **1000'** is divided into a plurality of areas and an additional data line for applying the PAM data voltage is provided for each area, an HDR may be realized for each of the plurality of areas even in one modular panel.

In the example described above, all transistors **311**, **312**, **315**, **321**, **322**, **323**, **325**, **331**, **332** and **361** included in the driving circuit **300** are implemented as a P-channel metal oxide semiconductor field effect transistor (PMOSFET), but are not limited thereto. However, example embodiments are not limited to any specific examples. According to an example embodiment, a driving circuit of which all transistors are implemented as an N-channel metal oxide semiconductor field effect transistor (NMOSFET) may be implemented to perform the same operation as the driving circuit **300** as described above.

The driving circuit including the NMOSFET may perform the same operation as the driving circuit **300** of FIG. **9** or **12**B except a difference due to a type of transistor (for example, a difference of connection relationship between devices and a difference of polarity of various signals to be applied). The operation of the driving circuit implemented as an NMOSFET through the description above would be easily understood by those skilled in the art based on a PMOSFET, and thus an unnecessary overlapping description will not be provided below.

FIG. **13** is a diagram illustrating a configuration of a display apparatus, according to an example embodiment. Referring to FIG. **13**, a display apparatus **1300** may include a display panel **1000** and **1000'**, a panel driver **800**, and a processor **900**.

The display panel **1000** and **1000'** may include a plurality of light emitting devices **200** included in a plurality of sub pixels, and a plurality of driving circuits **300** for driving the respective light emitting devices **200**.

For example, the display panel **1000** and **1000'** may be disposed such that gate lines G**1** to Gn and data lines D**1** to Dm intersect with each other, and the driving circuit **300** may be disposed in an area in which the intersection is provided. For example, the plurality of driving circuits **300** may be respectively configured such that adjacent R, G and B sub pixels form one pixel, but the example is not limited thereto.

The panel driver **800** may be controlled by the processor **900** to drive the display panel **1000** and **1000'** (in more detail, each of the plurality of driving circuits **300**), and may include a timing controller **810**, a data driver **820**, and a gate driver **830**.

The timing controller **810** may receive an input signal IS, a horizontal synchronizing signal Hsync, a vertical synchronizing signal Vsync and a main clock signal MCLK from the outside, and generate an image data signal, a scanning control signal, a data control signal, a data control signal, a light emission control signal, and the like to the display panel **1000** and provide the generated signals to the display panel **1000** and **1000'**, the data driver **820**, the gate driver **830**, and the like.

For example, according to various example embodiments, the timing controller **810** may apply at least one of various signals (Emi, Vsweep, Vini, VST and Test/Discharging) to the driving circuit **300**. According to an example embodiment, a control signal (MUX Sel R, G and B) for selecting one sub pixel from among the R, G and B sub pixels may be applied to the driving circuit **300**.

The data driver **820**, or source driver and data driver, may, as a means for generating a data signal, receive an image data of an R/G/B component from the processor **900** and generate a data voltage (for example, PWM data voltage and PAM data voltage). In addition, the data driver **820** may apply the generated data signal to the display panel **1000** and **1000'**.

The gate driver **830** (or gate driver) may, as a means for generating various control signals such as a control signal (SPWM(n)), a control signal (SPAM), and the like, transfer the generated various control signals to a particular row (or a particular horizontal line) of the display panel **1000** and **1000'** or to the entire lines.

In addition, the gate driver **830** may apply a driving voltage (VDD) to the driving voltage terminal of the driving circuit **300** according to an example embodiment.

Meanwhile, as described above, some or all of the data driver **820** and the gate driver **830** may be implemented to be included in the TFT layer **3000'** disposed on one surface of the glass **100** of the display panel **1000'** or implemented as an additional semiconductor integrated circuit (IC) and arranged on the other surface of the glass **100**.

The processor **900** may include various processing circuitry and controls overall operations of the display apparatus **1300**. In particular, the processor **900** may control the panel driver **800** to drive the display panel **1000** and **1000'** so that the driving circuit **300** performs the operations described above.

To this end, the processor **900** may include one or more of a central processing unit (CPU), micro-controller, application processor (AP), communication processor (CP), ARM processor, or the like.

For example, according to an example embodiment, the processor **900** may set a pulse width of a driving current according to a PWM data voltage, and control the panel driver **800** to set an amplitude of the driving current according to a PAM data voltage. In a case that the display panel **1000** and **1000'** includes a n number of columns and a m number of rows, the processor **900** may control the panel driver **800** to the PWM data voltage by the row (by the horizontal line). In addition, the processor **900** may control the panel driver **800** to apply the PAM data voltage at once to the entire sub pixels of the display panel **1000** and **1000'**.

Thereafter, the processor **900** may apply a driving voltage (VDD) at once to the plurality of driving circuits **300** and **700** included in the display panel **1000** and **1000'**, and control the panel driver **800** to apply a linear shift voltage (sweep signal) to a PWM driving circuit **320** of each of the plurality of driving circuits **300**, and thereby an image can be displayed.

In this case, the detail of the processor **900** controlling the panel driver **800** to control an operation of the respective driving circuits **300** included in the display panel **1000** and **1000'** is as described above and thus, the overlapped description will be omitted.

In FIG. **13**, the processor **900** and the timing controller **810** are separate elements. However, in an implementation, the timing controller **810** may perform a function of the processor **900** without the processor **900**.

FIG. **14** is a flowchart illustrating a method for driving a display apparatus, according to an example embodiment. In FIG. **14**, the same elements described above will not be described in detail.

According to an example embodiment, the display panel **1000** and **1000'** may be driven in the order of an initialization duration, a threshold voltage compensation duration, a data voltage setup duration, and a light emitting duration for one image frame.

Referring to FIG. **14**, the display panel **1000** and **1000'** may initialize voltages of gate terminals (nodes C and A) of the first and second driving transistors **311** and **321** of the PAM driving circuit **310** and the PWM driving circuit **320** during an initialization duration, at operation S**1410**. To stabilize the voltages of the node C and the node A, the display panel **1000** and **1000'** may first initialize voltages of nodes D and B, and then initialize the voltages of the nodes C and A.

Then, the display panel **1000** and **1000'** set a data voltage, and compensate threshold voltages of the first and second driving transistors **311** and **321**, at operation S1420. Here, the display panel **1000** and **1000'** may compensate the threshold voltages of the first and second driving transistors **311** and **321** based on the driving voltage (VDD) driving the driving circuit **300**.

For example, the display panel **1000** and **1000'** may compensate the threshold voltages of the first and second driving transistors **311** and **321** by applying a first voltage corresponding to the sum of the driving voltage (VDD) and the threshold voltage of the first driving transistor **311** to the node C, and applying a second voltage corresponding to the sum of the driving voltage VDD and the threshold voltage of the second driving transistor **321** to the node A.

Then, the display panel **1000** and **1000'** may set the PAM data voltage and the PWM data voltage to the PAM driving circuit **310** and the PWM driving circuit **320**, respectively, at operation S**1430**. For example, the display panel **1000** and **1000'** may apply a third voltage corresponding to the sum of the first voltage and the PAM data voltage to the node C, and apply a fourth voltage corresponding to the sum of the second voltage and the PWM data voltage to the node A, to set the data respectively.

The PWM data voltage may be applied for each of pixel lines included in the display panel **1000** and **1000'**, and the PAM data voltage may be applied at once to all pixels (or all sub pixels) included in the display panel **1000** and **1000'**.

Here, the PAM data voltage being "applied at once" to all the sub pixels included in the display panel **1000** and **1000'** does not necessarily mean that the PAM data voltage is "applied at the same time" to all the sub pixels included in the display panel **1000** and **1000'**.

That is, for example, in a case that a data line (Sig or PAM data (Block x)) is directly connected to all sub pixels included in the display panel **1000** and **1000'**, the voltage being "applied at once" may mean that the voltage is applied to all sub pixels at the same time.

However, in a case that the display panel **1000** and **1000'** is implemented in such a way that a PAM data voltage applied to pixels is time-divided through a MUX and applied to a sub pixel, the PAM data voltage is applied at once to the entire lines of the display panel **1000** and **1000'**, which does not necessarily mean that the voltage is applied to all sub pixels at the same time.

That is, a PAM data voltage being applied at once in the various example embodiments may mean that the PAM data voltage is applied at once to the entire lines rather than being sequentially applied for each line like the PWM data voltage (or the PAM data voltage in the external compensation method).

Accordingly, the display panel **1000** and **1000'** may express a grayscale or gradation by illuminating the light emitting device **200** through a driving current with amplitude corresponding to the PAM data voltage and a pulse width corresponding to the PWM data voltage, at operation **S1440**.

According to an example embodiment, the display panel **1000** and **1000'** may discharge an electrical charge remaining in the light emitting device **200** after the light emitting duration ends as described above.

In the example described above, the light emitting device **200** is a micro LED, but is not limited thereto. That is, according to an example embodiment, even when the light emitting device **200** is an LED of a size greater than or equal to 100 micrometers, the driving circuit **300** according to the various example embodiments described above may be applied.

In addition, in the example described above, the display panel **1000** and **1000'** is a chip-on-glass (COG) type, but the driving circuit **300** according to the various example embodiments described above may be applied to a display panel of a chip-on-board (COB) type. As for a display panel of a COB type, a substrate is used instead of the glass **100** unlike the COG type. In this case, a hole penetrating the substrate is formed and one surface of the substrate and the other surface of the substrate are electrically connected through the hole, and thereby the driving circuit **300** provided on one surface of the substrate and various circuits provided on the other surface of the substrate can be electrically connected to each other.

According to the various example embodiments, a wavelength shift of a light emitted from an inorganic light emitting device included in a display panel according to a grayscale or gradation can be prevented.

In addition, it is possible to correct a stain or color of the light emitting device included in the display panel, and even in a case that a large-area tiled display panel is configured by combining a display panel in the form of a plurality of modules, a difference of brightness or color among the respective modular display panels can be corrected.

Further, a more optimized driving circuit design is enabled so that the inorganic light emitting device can be driven more stably and efficiently, thereby contributing to a miniaturization and lightening of a display panel.

In addition, it is possible to realize an HDR by the magnitude desired by the engineer. In addition, a capacitor is not used in the internal compensation circuit and a coupling noise caused by a peripheral parasitic capacitance is eliminated, and thereby circuit driving performance can be improved.

Meanwhile, the above-described example embodiments may be implemented as an S/W program including an instruction stored on machine (e.g., computer)-readable storage media. The machine is an apparatus which is capable of calling a stored instruction from the storage medium and operating according to the called instruction, and may include a display apparatus **1200** according to the above-described example embodiments.

When the command is executed by a processor, the processor may perform a function corresponding to the command directly or using other components under the control of the processor. The command may include a code generated or executed by a compiler or an interpreter. A machine-readable storage medium may be provided in the form of a non-transitory storage medium. Herein, the term "non-transitory" only denotes that a storage medium does not include a signal but is tangible, and does not distinguish the case where a data is semi-permanently stored in a storage medium from the case where a data is temporarily stored in a storage medium.

According to an example embodiment, the method according to the above-described various example embodiments may be provided as being included in a computer program product. The computer program product may be traded as a product between a seller and a consumer. The computer program product may be distributed online in the form of machine-readable storage media (e.g., compact disc read only memory (CD-ROM)) or through an application store (e.g., Play Store™). In the case of online distribution, at least a portion of the computer program product may be at least temporarily stored or temporarily generated in a server of the manufacturer, a server of the application store, or a storage medium such as memory.

Each of the components (e.g., module or program) according to the various example embodiments may include a single entity or a plurality of entities, and some of the corresponding sub components described above may be omitted, or another sub component may be further added to the various example embodiments. Alternatively or additionally, some components (e.g., module or program) may be combined to form a single entity which performs the same or similar functions as the corresponding elements before being combined. Operations performed by a module, a program, or other component, according to various exemplary embodiments, may be sequential, parallel, or both, executed iteratively or heuristically, or at least some operations may be performed in a different order, omitted, or other operations may be added.

Although example embodiments of the present disclosure have been illustrated and described, it should be understood that the present disclosure is not limited to the disclosed embodiments and may be variously changed without departing from the spirit and the scope of the present disclosure. While the disclosure has been shown and described with reference to various embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the disclosure as defined by the appended claims and their equivalents. While the present disclosure has been shown and described with reference to various embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present disclosure as defined by the appended claims and their equivalents.

What is claimed is:

1. A display panel in which a plurality of pixels respectively including a plurality of sub pixels are arranged in a matrix form on a glass, wherein each of the plurality of sub pixels comprises:

a driving circuit disposed on the glass and configured to receive a pulse amplitude modulation (PAM) data voltage and a pulse width modulation (PWM) data voltage; and

an inorganic light emitting device mounted on the driving circuit and configured to be electrically connected to the driving circuit, and to emit a light based on a driving current provided from the driving circuit,

wherein the PAM data voltage is applied at once to the plurality of pixels included in the display panel, and

wherein the driving circuit is configured to control a grayscale of a light emitted by the inorganic light emitting device by compensating a deviation between driving circuits included in each of the plurality of sub pixels based on a driving voltage of the driving circuit and controlling a pulse width of a driving current having an amplitude corresponding to the applied PAM data voltage based on the applied PWM data voltage.

2. The display panel as claimed in claim **1**, wherein the driving circuit comprises:

a PAM driving circuit including a first driving transistor and configured to control an amplitude of the driving current based on the applied PAM data voltage; and

a PWM driving circuit including a second driving transistor and configured to control a pulse width of the driving current based on the applied PWM data voltage,

wherein the deviation between the driving circuits is a deviation of threshold voltage between first driving transistors included in each of the plurality of sub pixels, and a deviation of threshold voltage between second driving transistors included in each of the plurality of sub pixels.

3. The display panel as claimed in claim **2**, wherein the PAM driving circuit is configured to, based on the driving voltage being applied, apply a first voltage based on the driving voltage and a threshold voltage of the first driving transistor to a gate terminal of the first driving transistor, and

wherein the PWM driving circuit is configured to, based on the driving voltage being applied, apply a second voltage based on the driving voltage and a threshold voltage of the second driving transistor to a gate terminal of the second driving transistor.

4. The display panel as claimed in claim **2**, wherein the display panel is divided into a plurality of areas, and

wherein the PAM driving circuit receives the PAM data voltage for each of the plurality of areas.

5. The display panel as claimed in claim **4**, wherein a PAM data voltage applied to at least one area for driving a high dynamic range (HDR) from among the plurality of areas is different from a PAM data voltage applied to other areas of the plurality of areas.

6. The display panel as claimed in claim **3**, wherein the PAM driving circuit is configured to, after a gate terminal voltage of the first driving transistor being equal to the first voltage, based on the PAM data voltage being applied, apply a third voltage based on the first voltage and the PAM data voltage to the gate terminal of the first driving transistor,

wherein the PWM driving circuit is configured to, after a gate terminal voltage of the second driving transistor being equal to the first voltage, based on the PWM data voltage being applied, apply a fourth voltage based on the second voltage and the PWM data voltage to the gate terminal of the second driving transistor, and

wherein the driving circuit is configured to, based on the driving voltage being applied to the inorganic light emitting device through the first driving transistor and a linearly-changing sweep signal being applied to the PWM driving circuit, provide a driving current having an amplitude corresponding to the applied PAM data voltage to the inorganic light emitting device from a time when the driving voltage is applied to the inorganic light emitting device until a time when the fourth voltage applied to the gate terminal of the second driving transistor is linearly shifted according to the sweep signal and becomes the second voltage.

7. The display panel as claimed in claim **6**, wherein the PAM driving circuit includes a first transistor which is connected to and disposed between a drain terminal of the first driving transistor and the gate terminal of the first driving transistor;

a first capacitor including a first terminal commonly connected to a source terminal of the first driving transistor, a source terminal of the second driving transistor, and a driving voltage terminal of the driving circuit;

a second capacitor including a first terminal commonly connected to the gate terminal of the first driving transistor, a second terminal of the first capacitor, and a source terminal of the first transistor; and

a second transistor including a source terminal via which the PAM data voltage is applied, and a drain terminal connected to a second terminal of the second capacitor.

8. The display panel as claimed in claim **7**, wherein the PAM driving circuit is configured to:

while the first transistor is turned on, based on the driving voltage being applied via the driving voltage terminal, apply the first voltage corresponding to a sum of the driving voltage and the threshold voltage of the first driving transistor to the gate terminal of the first driving transistor via the turned-on first driving transistor; and

based on the PAM data voltage being applied via the source terminal of the second transistor, apply the third voltage corresponding to a sum of the first voltage and the applied PAM data voltage to a gate terminal of the first transistor.

9. The display panel as claimed in claim **7**, wherein the PWM driving circuit comprises:

a third transistor which is connected to in between a drain terminal of the second driving transistor and the gate terminal of the second driving transistor;

a fourth transistor including a drain terminal connected to the gate terminal of the second driving transistor and a source terminal of the third transistor;

a third capacitor including a first terminal commonly connected to the gate terminal of the second driving transistor, the source terminal of the third transistor, and the drain terminal of the fourth transistor;

a fifth transistor including a source terminal via which the PWM data voltage is applied, and a drain terminal connected to a second terminal of the third capacitor; and

a fourth capacitor including a first terminal commonly connected to the second terminal of the third capacitor and the drain terminal of the fifth transistor, and a second terminal receiving a linearly-shifting sweep signal.

10. The display panel as claimed in claim **9**, wherein the PWM driving circuit is configured to:

while the third transistor is turned on, based on the driving voltage being applied via a the driving voltage terminal, apply the second voltage corresponding to a sum of the driving voltage and the threshold voltage of the second driving transistor to the gate terminal of the second driving transistor via the turned-on second driving transistor; and

based on the PWM data voltage being applied via the source terminal of the fifth transistor, apply the fourth voltage corresponding to the second voltage and the applied PWM data voltage to the gate terminal of the second transistor.

11. The display panel as claimed in claim **9**, wherein the driving circuit further comprises:

a sixth transistor including a source terminal commonly connected to the drain terminal of the second driving transistor and a drain terminal of the third transistor, and a drain terminal commonly connected to the gate terminal of the first driving transistor, the second terminal of the first capacitor, the first terminal of the second capacitor, and the source terminal of the first transistor; and

a seventh transistor including a source terminal commonly connected to the drain terminal of the first driving transistor and a drain terminal of the first transistor, and a drain terminal connected to an anode terminal of the light emitting device,

wherein a cathode terminal of the inorganic light emitting device is connected to a ground voltage terminal of the driving circuit.

12. The display panel as claimed in claim **11**, wherein the driving circuit is configured to:

drive the PAM driving circuit and the PWM driving circuit independently of each other while the sixth and seventh transistors are turned off, and apply the first voltage and the second voltage to the gate terminal of the first driving transistor and the gate terminal of the second driving transistor, respectively; and

while the sixth and seventh transistors are turned on, based on the sweep signal being applied via the fourth capacitor, drive the PAM driving circuit and the PWM driving circuit together, and until the fourth voltage applied to the gate terminal of the second driving transistor is shifted according to the sweep voltage and becomes the second voltage, provide a driving current having an amplitude corresponding to the applied PAM data voltage to the inorganic light emitting device.

13. The display panel as claimed in claim **11**, wherein gate terminal voltages of the first and second driving transistors are, before the first and second voltages are respectively applied, initialized based on an initial voltage applied via the fourth transistor turned on while the sixth and seventh transistors are turned on.

14. The display panel as claimed in claim **11**, wherein the driving circuit further comprises:

an eighth transistor which is connected to and disposed between the anode terminal of the inorganic light emitting device and the cathode terminal of the inorganic light emitting device.

15. The display panel as claimed in claim **14**, wherein the eighth transistor is configured to:

before the inorganic light emitting device is mounted on the driving circuit, be turned on to check whether the driving circuit is abnormal; and

after the inorganic light emitting device is mounted on the driving circuit, be turned on to discharge an electric charge remaining in the inorganic light emitting device.

16. The display panel as claimed in claim **1**, wherein the PWM data voltage is sequentially applied to the plurality of pixels for each line of the plurality of pixels arranged in the matrix form.

17. The display panel as claimed in claim **1**, wherein the PAM data voltage applied at once to the plurality of sub pixels is a voltage of a same magnitude.

18. The display panel as claimed in claim **1**, wherein the plurality of sub pixels include an R sub pixel including an inorganic light emitting device emitting a red (R) light, a G sub pixel including an inorganic light emitting device emitting a green (G) light, and a B sub pixel including an inorganic light emitting device emitting a blue (B) light.

19. The display panel as claimed in claim **1**, wherein the inorganic light emitting device is a micro-LED having a size of less than or equal to 100 micrometers.

20. A method for driving a display panel comprising a plurality of pixels respectively including a plurality of sub pixels arranged in a matrix form on a glass, wherein each of the plurality of sub pixels comprises:

a driving circuit formed on the glass and configured to receive a pulse amplitude modulation (PAM) data voltage and a pulse width modulation (PWM) data voltage; and

an inorganic light emitting device mounted on the driving circuit and configured to be electrically connected to the driving circuit, and to emit a light based on a driving current provided from the driving circuit,

wherein the method comprises:

compensating a threshold voltage of a driving transistor included in the driving circuit based on a driving voltage of the driving circuit;

setting the applied PAM data voltage and the applied PWM data voltage; and

providing, to the inorganic light emitting device, a driving current having an amplitude corresponding to the applied PAM data voltage and a pulse width corresponding to the applied PWM data voltage,

wherein the PAM data voltage is applied at once to the plurality of pixels included in the display panel.

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其他公开文献	US20200111403A1
外部链接	Espacenet

摘要(译)

提供显示面板。 在显示面板中,分别包括多个子像素的多个像素以矩阵形式布置在玻璃上。 多个子像素中的每一个包括:驱动电路,其布置在玻璃上并被配置为接收PAM数据电压和PWM数据电压;以及无机发光器件,其被配置为基于从驱动电路提供的驱动电流来发光。 。 将PAM数据电压立即施加到显示面板中包括的多个像素。 驱动电路基于驱动电路的驱动电压补偿包括在多个子像素中的每个子像素中的驱动电路之间的偏差,并且基于驱动电路来控制具有与所施加的PAM数据电压相对应的幅度的驱动电流的脉冲宽度。 施加的PWM数据电压。